Modeling, Control, and Protection of Multi-Terminal DC Transmission for Improving Power Grid's Performance

Final Project Report

S-76

Power Systems Engineering Research Center

Empowering Minds to Engineer
the Future Electric Energy System

Modeling, Control, and Protection of Multi-Terminal DC Transmission for Improving Power Grid's Performance

Final Project Report

Project Team

Maryam Saeedifard, Project Leader
Georgia Institute of Technology

Jiangchao Qin
Arizona State University

Ali Mehrizi-Sani
Washington State University

Graduate Students

Jingfan Sun
Mahmoud MehrabanKhomartash
Georgia Institute of Technology

Yuntao Zou
Arizona State University

Armin Teymouri
Washington State University

PSERC Publication 19-05

October 2019

For information about this project, contact:

Maryam Saeedifard
Georgia Institute of Technology
777 Atlantic Dr.
Atlanta, GA 30308
Phone: 404-894-4834
Email: Maryam@ece.gatech.edu

Power Systems Engineering Research Center

The Power Systems Engineering Research Center (PSERC) is a multi-university Center conducting research on challenges facing the electric power industry and educating the next generation of power engineers. More information about PSERC can be found at the Center's website: http://www.pserc.org.

For additional information, contact:

Power Systems Engineering Research Center
Arizona State University
527 Engineering Research Center
Tempe, Arizona 85287-5706
Phone: 480-965-1643
Fax: 480-727-2052

Notice Concerning Copyright Material

Acknowledgements

We wish to thank Ms. Ying Song from Xi'an Jiaotong University who visited our lab at Georgia Tech and collaborated with the Ph.D. student, Jingfan Sun on a part of this work. We express our appreciation for the support provided by PSERC industry members: Rambabu Adapa (EPRI), Neil Kirby (GE Energy Connections), Harvey Scribner (SPP), Reynaldo Nuqui (ABB), Innocent Kamwa (Institut de Recherche d'Hydro-Québec), Saman Babaei (NYPA), Alan Ettlinger (NYPA), Eduard Muljadi (NREL), Di Shi (Global Energy Interconnection Research Institute North America), and Jiuping Pan (ABB).

Special thanks are also due to Harvey Scribner (SPP), Rambabu Aadapa (EPRI), Jiuping Pan (ABB), and Di Shi (GEIRI North America) for their constructive comments and feedbacks on improving the quality of this work and report.

Executive Summary

High Voltage DC (HVDC) transmission is a long-standing technology with many installations around the world. Over the past few years, significant breakthroughs in the Voltage-Sourced Converter (VSC) technology along with their attractive features have made the HVDC technology even more promising in providing enhanced reliability and functionality and reducing cost and power losses. Concomitantly, significant changes in generation, transmission, and loads such as (i) integration and tapping renewable energy generation in remote areas, (ii) need for relocation or bypassing older conventional and/or nuclear power plants, (iii) increasing transmission capacity, and (iv) urbanization and the need to feed the large cities have emerged. These new trends have called for Multi-Terminal DC (MTDC) systems, which when embedded inside the AC grid, can enhance stability, reliability, and efficiency of the present power grid. Amid the optimism surrounding the MTDC grids, the following fundamental research questions must be addressed (i) what control strategies are required to operate the MTDC converter stations, (ii) how will the MTDC grid interact with its surrounding AC system and what kind of services (e.g., frequency support and power oscillation damping) can it provide, (iii) how can DC faults be detected, identified, and cleared. To this end, a multi-pronged research effort is proposed: (i) Development of suitable dynamic models of the MTDC systems, which can be efficiently solved together with the AC systems; (ii) Design of advanced control strategies enabling the MTDC systems to support the resulting hybrid AC/DC systems; and (iii) Development of strategies for DC fault detection, identification, and protection of MTDC systems.

Part I – 1. Backup Protection of Multi-Terminal HVDC Grids Based on Quickest Change Detection

Amid the optimism surrounding the benefits of MTDC grids, their protection against DC-side faults remains one of their major technical challenges. MTDC grid protection is far more difficult than AC grids as DC fault phenomenon is more complex. The protection philosophy of the MTDC grids, nevertheless, is similar to the AC counterparts in the sense that both primary and backup protection schemes are required. In case the primary protection fails to act properly, backup protection should trip as quickly as possible to minimize the loss of power in-feed. In this part, a new backup protection algorithm based on quickest change detection (QCD) method is proposed for MTDC grids. In backup protection settings, the signals from voltage measurements are observed by a decision maker, which monitors any abrupt change in the voltage distribution using sequential measurements. The objective is to detect the change as fast as possible subject to a constraint on the false alarm rate. With sequentially monitoring of signals, the QCD method proposed here is able to quickly trip the breakers under noisy signals with a negligible computation effort. The method is applicable to general N-terminal MTDC grids.

Part I – 2. Reducing the Fault Transient Magnitudes in Multi-terminal HVDC Grids by Sequential Tripping of Hybrid Circuit Breaker Modules

Proper protection of the MTDC grids necessitates the DC circuit breakers (CBs) to selectively and quickly isolate any faulty line without interrupting the entire system. Among the proposed DC CBs, the hybrid solid-state one is the most promising option as its breaking time is in the

order of a few milliseconds while its conduction losses during normal operation are quite low. To speed up the operation of hybrid DC CB and attenuate over-currents and over-voltages, a sequential switching strategy is proposed in this part. This switching strategy enables a step-by-step tripping of breaker modules even before the ultra-fast disconnect switch is fully opened. Based on the proposed approach, the fault is interrupted in an early stage by applying the voltage of the arrester banks within each breaker module in a progressive manner. This earlier interruption of fault reduces the rate of rise of fault current and, consequently, contributes to the attenuation of the overcurrent and overvoltage stresses as well as shorter fault clearance time. To verify the benefits of the proposed sequential switching strategy, performance metrics indicating the current and voltage stresses are quantified through a time-domain analytical modeling approach considering travelling waves on DC transmission lines. The transient performance of the sequential tripping mechanism is confirmed based on both simulation studies in the PSCAD/EMTDC software environment and quantitative analysis.

Part I – 3. Optimum Selection of Circuit Breaker Parameters based on Analytical Calculation of Overcurrent and Overvoltage in Multi-terminal HVDC Grids

Incorporating hybrid DC CBs into the MTDC grid adds another level of complexity as the DC short circuit current increases with commensurate increase in transient overvoltage stress, current limiting reactor and energy absorption capability of arresters. To determine the fault clearing capability and performance of these DC breakers, there is a need for (i) an accurate method to estimate the maximum overcurrent, transient overvoltage stress and energy absorption, and (ii) an optimal parameter selection method to size the CB components to achieve satisfactory performance. Once a quantitative estimation of maximum fault current, overvoltage, clearance time and energy absorption in arresters is obtained, optimum selection of the CB components can be attained. In this part, a time-domain approach is proposed to analytically calculate the transient response of the MTDC system during a DC fault by considering all the corresponding travelling waves. Based on the analysis, the fault behavior within the first few milliseconds is analytically modelled, and consequently, breaker parameters including operation delay, current limiting reactor and arrester can be optimally sized. In that regard, a multi-objective design optimization problem is formulated to explore the Pareto-optimal fronts of the transient response of the system versus the breaker parameters and to establish trade-offs among the breaker parameters and fault transient response. Finally, time-domain simulations in the PSCAD/EMTDC environment are performed to evaluate the accuracy and performance of the proposed method.

Part I – 4. Model Predictive Control-Based AC Line Overload Alleviation in Meshed AC/MTDC Grids

MTDC grids can support the future AC grid by improving its frequency response of the AC grid, inter-area oscillation damping, and reducing the operational cost of the electricity grid. In addition to the aforementioned functions, a MTDC grid can play a major role in AC line overload alleviation. The contribution of this part is a Model Predictive Control (MPC)-based strategy, which uses MTDC converter stations along with the AC grid generators for transmission line overload alleviation. The objective is to reduce active powers of the overloaded AC lines by deploying the MTDC converters and AC generators. The advantage of the proposed

controller is to simultaneously use the MTDC converter stations and AC system generators to relieve the overloads of AC lines. The proposed controller is integrated with the conventional Automatic Generation Control (AGC), thereby following a contingency, the system regulates frequency and mitigates AC line overloads, simultaneously. The controller receives the measurements within regular sampling time periods. When an outage imposes overloads on AC lines, the controller computes and dispatches the optimum setpoints of the active powers of the MTDC converters and the AC grid generators within each sampling time period. The optimum setpoints are computed by a MPC strategy to bring the active powers of the overloaded AC lines below their limits. To implement the MPC strategy, the sensitivity matrices relating the AC line active powers, DC line currents and DC bus voltages to the converters' active power setpoints and the generator active powers are calculated. Furthermore, all the operational constraints including constraints of the DC bus voltages, the DC line currents, the ratings of the MTDC converter stations, AC bus voltages, and the ramp rates are meticulously considered. The proposed controller constantly checks a voltage stability criterion to ensure that it does not push the system towards the voltage instability boundaries. The performance of the proposed controller is evaluated and demonstrated using time-domain simulation studies on two test systems, i.e., the 39-bus New England test system integrated with a 5-bus MTDC grid and the IEEE 118-bus test system integrated with a 6-bus MTDC grid.

Part II: A Hybrid Nonlinear Droop Control for MTDC Systems with Improved Dynamic Performance and Stability

Droop control is extensively applied to MTDC systems. However, in the case of large active power disturbance, the constant derivative of the linear droop curve leads to large voltage deviation and longtime regulation. In this part, a hybrid droop control is proposed with a cubic accelerated term and reference self-correction algorithm for voltage source converter-based MTDC systems. The proposed method can improve performance of the MTDC systems during transient and steady-state operations. The cubic accelerated term can provide fast regulation speed and low voltage deviation during transient due to the proposed nonlinear droop curve. The reference self-correction algorithm is developed to move the curve to the new operating point for eliminating voltage deviation and maintaining the constant dynamic performance. In the steady state, the proposed droop curve is approximated to a linear one by neglecting the cubit accelerated term due to its much smaller value. Therefore, the negative influences of the conventional nonlinear droop curve on regulation speed, voltage deviation, and power oscillation can be avoided. The simulation results of a four-terminal system in the PSCAD/EMTDC software environment demonstrate the effectiveness of the proposed droop control.

Part III: Feedforward Accurate Power Sharing and Voltage Control for Multi-Terminal HVDC Grids

This part presents a power sharing and voltage control scheme for MTDC grids. A generalized hierarchical droop-based controller is designed to control the DC-side voltages and dispatched powers. To improve the steady-state performance of the MTDC grid, this project proposes a feedforward mechanism to make the current controller of the voltage-sourced converters independent of the AC-side load conditions. The performance of the proposed scheme is evaluated under several case studies. A comparison between the proposed controller and

traditional controllers is also made with time-domain simulation studies in PSCAD/EMTDC software. Results show that the proposed controller can successfully control the real powers and DC voltages while having a stable performance during AC-side load changes.

Project Publications:

[1] Y. Song, J. Sun, M. Saeedifard, S. Ji, L. Zhu, A.P. Meliopoulos, and L. Graber, "Optimum Selection of Circuit Breaker Parameters based on Analytical Calculation of Overcurrent and Overvoltage in Multiterminal HVDC Grids," *IEEE Trans. on Industrial Electronics*. Accepted.

[2] M. Mehraban, M. Saeedifard, and S. Grijalva, "Model Predictive Control-Based Thermal Overload Alleviation in Meshed AC/MTDC Grids," *IEEE Trans. on Power Systems*. Accepted.

[3] Y. Song, J. Sun, M. Saeedifard, S. Ji, L. Zhu, A.P. Meliopoulos, and L. Graber, "Reducing the Fault Transient Magnitudes in Multi-terminal HVDC Grids by Sequential Tripping of Hybrid Circuit Breaker Modules," *IEEE Trans. on Industrial Electronics,* vol. 66, no. 9, pp. 7290-7299, 2019.

[4] J. Sun, M. Saeedifard, and A.P. Meliopoulos, "Backup Protection of Multi-terminal HVDC Grids Based on Quickest Change Detection," *IEEE Trans. on Power Delivery*. vol. 34, no. 1, pp.177-187, 2019.

[5] J. Sun, M. Saeedifard, and AP. Meliopoulos, "Sequential Tripping of Hybrid DC Circuit Breakers to Enhance the Fault Interruption Capability in Multi-Terminal DC Grids," CIGRE US National Committee 2018 Grid of the Future Symposium, October 2018.

[6] M. Mehrabankhomartash and M. Saeedifard, "The Impact of Multi-Terminal DC Grids on AC Line Overload Alleviation: A Model Predictive Approach," IEEE Energy Conversion Conference and Exposition, 2019.

[7] Y. Zou and J. QIn, "A Hybrid Nonlinear Droop Control for MTDC Systems with Improved Dynamic Performance and Stability," IEEE Trans., in preparation.

Student Theses:

[1] Jingfan Sun, Protection of Multi-Terminal HVDC Grids, Ph.D, Georgia Institute of Technology, May 2020 (expected).

[2] Mahmoud MehrabanKhomartash, Control and Coordination of Multi-Terminal HVDC Grids, Georgia Institute of Technology, May 2021 (expected).

[3] Yuntao Zou. Control and Stability of MTDC Systems and DC Grids. Ph.D. dissertation, Arizona State University, May 2021(expected).

Part I

Modeling, Control, and Protection of Multi-Terminal DC Transmission for Improving Power Grid's Performance

Maryam Saeedifard
Jingfan Sun
Mahmoud MehrabanKhomartash

Georgia Institute of Technology

For information about this project, contact:

Maryam Saeedifard
Georgia Institute of Technology
777 Atlantic Dr.
Atlanta, GA 30308
Phone: 404-894-4834
Email: Maryam@ece.gatech.edu

Power Systems Engineering Research Center

The Power Systems Engineering Research Center (PSERC) is a multi-university Center conducting research on challenges facing the electric power industry and educating the next generation of power engineers. More information about PSERC can be found at the Center's website: http://www.pserc.org.

For additional information, contact:

Power Systems Engineering Research Center
Arizona State University
527 Engineering Research Center
Tempe, Arizona 85287-5706
Phone: 480-965-1643
Fax: 480-727-2052

Notice Concerning Copyright Material

Table of Contents

1. Backup Protection of Multi-Terminal HVDC Grids Based on Quickest Change Detection.... 1
   - 1.1 Introduction....1
   - 1.2 Test Multi-terminal HVDC System....2
   - 1.3 The Proposed Backup Protection Algorithm....3
     - 1.3.1 Layout of the Protection Unit....3
     - 1.3.2 The Proposed QCD Algorithm....4
     - 1.3.3 Backup Protection for Breaker Failure....8
     - 1.3.4 Backup Protection for Relay Failure....9
     - 1.3.5 Overall Protection Scheme....10
   - 1.4 Simulation Results....10
     - 1.4.1 Base Case....10
     - 1.4.2 Compatability with Different Breaker Configuration....19
     - 1.4.3 Blocking of IGBTs....19
     - 1.4.4 Low-Impedance Pole-to-ground Fault....19
     - 1.4.5 High-Impedance Pole-to-ground Fault....20
     - 1.4.6 Reversed Power Flow....20
     - 1.4.7 Comparison with the Existing Methods....20
   - 1.5 Conclusion....23
   - A. Proof of the Equivalence of g_k and g_k^m....25
   - B. Derivation of The Recursive Form of g_k....26
2. Reducing the Fault Transient Magnitudes in Multi-terminal HVDC Grids by Sequential Tripping of Hybrid Circuit Breaker Modules....27
   - 2.1 Introduction....27
   - 2.2 The Proposed Sequential Switching....28
   - 2.3 Energy distribution among arresters....32
   - 2.4 Tripping signal optimization....33
     - 2.4.1 Approach 1....34
     - 2.4.2 Approach 2....36
   - 2.5 Time-domain Transient Calculation....36
   - 2.6 Results....46
     - 2.6.1 Base Case....47

2.6.2 Modified Sequential Case....48
2.6.3 Optimized Sequential Strategy....48
2.7 Conclusion....49
3. Optimum Selection of Circuit Breaker Parameters based on Analytical Calculation of Overcurrent and Overvoltage in Multi-terminal HVDC Grids....51
3.1 Introduction....51
3.2 Test Multi-terminal HVDC System....52
3.3 Analytic Fault Transient Approximation....53
3.3.1 Frequency-domain Expression of traveling Waves....53
3.3.2 Time-domain Estimation of Traveling Waves....56
3.3.3 Estimation of the Worst-case Fault Location....60
3.4 Parameter Optimization....62
3.5 Study Results....64
3.5.1 Evaluation of the Transient Analysis....64
3.5.2 Optimum Parameter Selection of the Breaker....66
3.6 Conclusion....68
4. Model Predictive Control-Based AC Line Overload Alleviation in Meshed AC/MTDC Grids....69
4.1 Introduction....69
4.2 The Proposed Method....70
4.3 Simulation Results....77
4.3.1 Test System 1....77
4.3.2 Scenario a....79
4.3.3 Scenario b....80
4.3.4 Scenario c....81
4.3.5 Test System 2....82
4.3.6 Comparison with the conventional method....87
4.3.7 Influence of weighting factors....87
4.3.8 Possible limitations of the MTDC grid....91
4.4 Conclusion....92
References....93

List of Figures

Figure 1.1 Layout of the four-terminal HVDC grid test system [14] 2

Figure 1.2 Diagrams of MMC models and intenal protection. a) submodeules (SMs) in a MMC arm; b) continuous equivalent MMC arm model with blacking/de-blocking capabilities [14] [21]; and c) MMC internal overcurrent and under-voltage protection 3

Figure 1.3 Hybrid HVDC circuit breaker adopted in this study 4

Figure 1.4 The proposed layout of the protection unit at Bus *i* 5

Figure 1.5 Simulated transients of the hybrid circuit breaker CB_{13p} under a pole-to-pole fault in the middle of Line13. a) auxiliary branch, main breaker and arrester currents; and b) voltage across the breaker 8

Figure 1.6 Breaker failure backup protection scheme 9

Figure 1.7 Simulation results with a pole-to-pole fault in the middle of Line13, under both successful breaker operation and breaker failure; (a) voltage across circuit breaker v_{cb13p}, (b) current flowing through circuit breaker i_{cb13p}, (c) zoomed-in portion of outputs from beaker failure QCD alogrithm, and (d) outputs of AND gates 1, 2, and 3 from Figure 1.6..... 11

Figure 1.8 Simulation results with a pole-to-pole fault in the middle of Line13, under both normal and faulty conditions: (a) v^{l13}, voltage of Line13 at Bus 1, (b) outputs from beaker relay backup algorithm, (c) and (d) zoomed-in portion of (a) and (b), respectively 12

Figure 1.9 Simulation results with different breaker configurations: (a) voltage across the circuit breaker v_{cb13p}, (b) current flowing through the circuit breaker i_{cb13p}, (c) outputs of the beaker failure QCD algorithm under successful breaker operation for breaker 1, (d) outputs of the beaker failure QCD algorithm under successful breaker operation for breaker 2 13

Figure 1.10 Simulation results of converter internal protection quantities with a pole-to-pole fault in the middle of Line13: (a) upper arm currents of MMC1, (b) lower are currents of MC1, (c) DC voltage on MMC1 terminal side and MMC3 terminal side (for undervoltage interal protection), (d) blocking signalds of MMC1 and MMC2, (e) voltage across the circuit breaker v_{cb13p} with and without converter blocking enabled, and (f) v^{l13}, voltage of Line13 at Bus 1 with and without converter blocking enabled..... 14

Figure 1.11 Simulation results with a low-impedance fault in the middle of Line13: (a) voltage across the circuit breaker v_{cb13p}, (b) outputs of the beaker failure QCD algorithm under successful breaker operation, (c) v^{l13}, voltage of Line13 at Bus 1, (d) ooutputs of the relay failure backup algorithm during the fault, and (e) arm currents of MMC1, and positive pole current of Line13 i^{l13p}..... 15

Figure 1.12 Simulation results with a high-impedance fault in the middle of Line13: (a) voltage across the circuit breaker v_{cb13p}, (b) outputs of the beaker failure QCD algorithm under successful breaker operation, (c) v^{l13}, voltage of Line 13 at Bus 1, (d) outputs of the relay failure backup algorithm during the fault, and (e) arm currents of MMC1, and positive pole current of Line13 i^{l13p}..... 16

Figure 1.13 Simulation results under reversed power flow: (a) voltage across the circuit breaker v_{cb13p}, (b) outputs of the beaker failure QCD algorithm under successful breaker

operation, (c) v^{l13}, voltage of Line13 at Bus 1, (d) outputs of the relay failure backup algorithm during the fault, and (e) arm currents of MMC1, and positive pole curent of Line13 i^{l13p} 17

Figure 1.14 Comparison under noise. (a) voltage across the circuit breaker v_{cb13p}, (b) v^{l13}, voltage of Line13 at Bus 1, (c) and (d) results from the proposed and classifier-based methods, and (e) decision variables 21

Figure 1.15 Comparison under spike. (a) voltage across the circuit breaker v^{cb13p}, (b) v^{l13}, voltage of Line13 at Bus 1, (c) and (d) results from the proposed and classifier-based method, and (e) decision variables 22

Figure 2.1 Circuit diagram of the hybrid DC circuit breaker [5] 28

Figure 2.2 Simulated results in simultaneous and sequential tripping cases: a) voltage of the hybrid CB; and b) fault current 30

Figure 2.3 Simulated results of each module: a) currents of each module; b) voltage of various module arresters; c) absorbed energy by arresters and d) V-I characteristic of the arrester 31

Figure 2.4 Generic voltage withstand capability versus opening time of the UFD 34

Figure 2.5 Equivalent circuit of the terminal of the faulty line 38

Figure 2.6 Layout of the five-terminal HVDC system [18, 19] 39

Figure 2.7 Transients of simultaneous and sequential tripeed hybrid CBs: a) bus-side voltage of the breaker, b) fault current, c) absorbed energy of arresters for simultaneous case and d) absorbed energy of arresters of sequential case 40

Figure 2.8 Transients of the modified sequentially tripped hybrid CB: a) bus-side voltage, b) fault current and c) absorbed energy 41

Figure 2.9 Fault transient performance variation versus u_r and N: a) maximum fault current, b) maximum overvoltage c) clearance time and d) absorbed energy 42

Figure 2.10 Simulation results of the selected scenarios: a) fault current, b) bus-side voltage, c) absorbed energy in scenario (i), d) absorbed energy in scenario (ii), and e) absorbed energy with updated time instants 43

Figure 2.11 Fault transient performance variation versus u_{r1} and u_{r2}: a) maximum fault current, b) maximum overvoltage c) clearance time and d) absorbed energy 44

Figure 2.12 Simulation results of the selected scenarios: a) fault current, b) bus-side voltage c) absorved energy in scenario (i), and d) absorbed energy in scenario (ii) 46

Figure 3.1 a) Layout of the MTDC grid test system and b) circuit diagram of the hybrid CB with its three paths 53

Figure 3.2 Fault current contributions during a pole-to-pole fault at Bus_i 54

Figure 3.3 Lattice diagram for traveling waves of a faulty cable 55

Figure 3.4 a) Equivalent DC circuit under a pole-to-pole fault; and b) the reflection co-efficient at the terminal of the faulty cable 57

Figure 3.5 Conducting arms of the MMC: a) Stage 1B and b) Stage 1C 58

Figure 3.6 The waveforms during DC breaker operation: a) current on each branch of DC CB and b) bus-side voltage of DC CB 58

Figure 3.7 Equivalent DC circuits of a pole-to-pole fault: a) Stages 1B and 1C; and b) Stage 2 59

Figure 3.8 Voltage at the terminal of the faulty cable with different fault location 60

Figure 3.9 Calculated and simulated results: Case 1: a) calculated currents; b) simulated currents; c) fault current $i_{f,43}$; d) cable-side voltage v_{41}; and e) the bus-side voltage v_{42}; Case 2: f) calculated currents; g) fault current $i_{f,54}$; h) bus-side voltage v_{52}; and i) energy absorption W_{EAP} 62

Figure 3.10 Calculated results for I_{max}, $V_{max,}$ t_{clear} and W_{EAP} with one parameter being changed: (a-1)-(a-4) objectives vary with L_{cb}; (b-1)-(b-4) objectives vary with t_{delay}; and (c-1)-(c-3) objectives vary with U_r 65

Figure 3.11 Pareto-optimal front of the feasible objective space 67

Figure 4.1 A typical MTDC grid embedded in an AC grid 71

Figure 4.2 Overall block diagram representation of the proposed controller 72

Figure 4.3 The influence of the fourth and fifth terms in (2.4): (a) penalty function corresponding to an AC line constratint, (b) penalty function corresponding to a DC line constraint 74

Figure 4.4 The New England 39-bus test system embedded with a 5-bus MTDC system 78

Figure 4.5 System response to the outage of line L15 – 16: O. I.s of the AC lines 79

Figure 4.6 System response to the outage of line L15 – 16: (a) AC system generator active powers, and (b) MTDC converter active powers injected into the AC grid 80

Figure 4.7 System response to the outage of line L15 – 16: (a) DC bus voltages, and (b) DC line currents 81

Figure 4.8 System response to the outage of line L15 – 16: share of the MTDC converters and the AC system generators in the AC line active power changes from t = 0 s to t = 200 s 82

Figure 4.9 System response to energization of a load at bus 16: (a) O. I.s of the AC lines, and (b) frequency of the AC system 83

Figure 4.10 System response to energization of a load at bus 16: (a) active pwoers of the MTDC converters, (b) DC bus voltages, and (c) DC line currents 84

Figure 4.11 Active powers of the MTDC converters following the outage of MMC3 84

Figure 4.12 System response to the outage of MMC3: (a) O. I.s of lines L2 – 3 and L16 – 19, (b) DC bus voltages, and (c) DC line currents 85

Figure 4.13 A 6-bus MTDC system embedded within the IEEE 118-bus test system 85

Figure 4.14 Comparison between the proposed and conventional methods: (a) O. I.s of the AC lines, (b) O. I. of line L17 – 30, (c) O. I. of line L38 – 65, and (d) O. I. of line L77 – 78 86

Figure 4.15 Influence of the weighting factors: (a) O. I.s of the AC lines in Case 1, (b) O. I.s of the AC lines in Case 2, and (c) O. I.s of the AC lines in Case 3 89

Figure 4.16 Influence of the weighting factors: (a) setpoint changes of the MTDC converter stations in Case 1, (b) setpoint changes of the MTDC converter stations in Case 3, (c) setpoint changes of the AC generators in Case1, and (d) set-point changes of the AC generators in Case 3 90

Figure 4.17 Simultaneous DC line and AC line overloads: (a) current of the DC line connecting MMC4 to MMC5, and (b) O. I.s of the AC lines 91

Figure 4.18 AC bus voltage constraint and voltage stability: (a) AC bus voltages, and (b) voltage stability criterion 92

List of Tables

Table 2.1 Demonstration of the modified sequential tripping strategy [13] 33
Table 2.2 Converter and grid parameters 47
Table 2.3 Absorbed energy by arresters 48
Table 3.1 Converter and grid parameters 64
Table 3.2 Selected parameters for optimized objectives 67
Table 4.1 Three case scenarios with different weighting factors 88

1. Backup Protection of Multi-Terminal HVDC Grids Based on Quickest Change Detection

1.1 Introduction

High Voltage DC (HVDC) transmission is a mature technology with many installations around the world [1]- [3]. Over the past few years, significant breakthroughs in Voltage-Sourced Converters (VSCs) along with their attractive features have made the HVDC technology even more promising in providing enhanced reliability and functionality and reducing cost and power losses. Concomitantly, significant changes in generation, transmission, and loads such as integration and tapping renewable energy generation in remote areas, the need for relocation or bypassing older conventional and/or nuclear power plants, increasing transmission capacity, urbanization and the need to feed the large cities have emerged [2]. These new trends have called for Multi-Terminal DC (MTDC) systems, which when embedded inside the AC grid, can enhance stability, reliability, and efficiency of the present power grid [1].

Amid the optimism surrounding the benefits of MTDC grids, their protection against DC-side faults remains one of their major technical challenges. MTDC grid protection is far more difficult than AC grids as DC fault phenomenon is more complex. The protection philosophy of the MTDC grids, nevertheless, is similar to the AC counterparts in the sense that both primary and backup protection schemes are required. In case the primary protection fails to act properly, backup protection should trip as quickly as possible to minimize the loss of power in-feed [5].

In the technical literature, the following backup protection algorithms have been proposed for HVDC grids [6]- [9]:

- A current threshold-based algorithm [6] in which the breaker failure is identified after a certain time delay following the trip signal from primary protection. To avoid misdetection in backup protection, the time interval is selected to be 20 ms. This results in a low detection speed and high ratings of circuit breakers.
- A local backup protection algorithm [7] [8] in which classifiers are designed to detect primary protection failure using voltage-current signals from corresponding relays. The uncleared and cleared faults are distinguished by a decision boundary on the voltage-current curve found by a classifier, which is trained using a large amount of data. The robustness of this method is evaluated in [9] under various system conditions and operating delays. Although the speed of this algorithm is faster than the previous current based method, it has the following drawbacks: a) detailed system modeling and accurate measurements are required to find an accurate boundary; b) the classifier has to be trained with lots of pre-acquired data under various conditions including different fault locations, fault impedance, and power flow; c) the scalability of this method is limited because the classifier has to be reset to be used in modified system topologies.

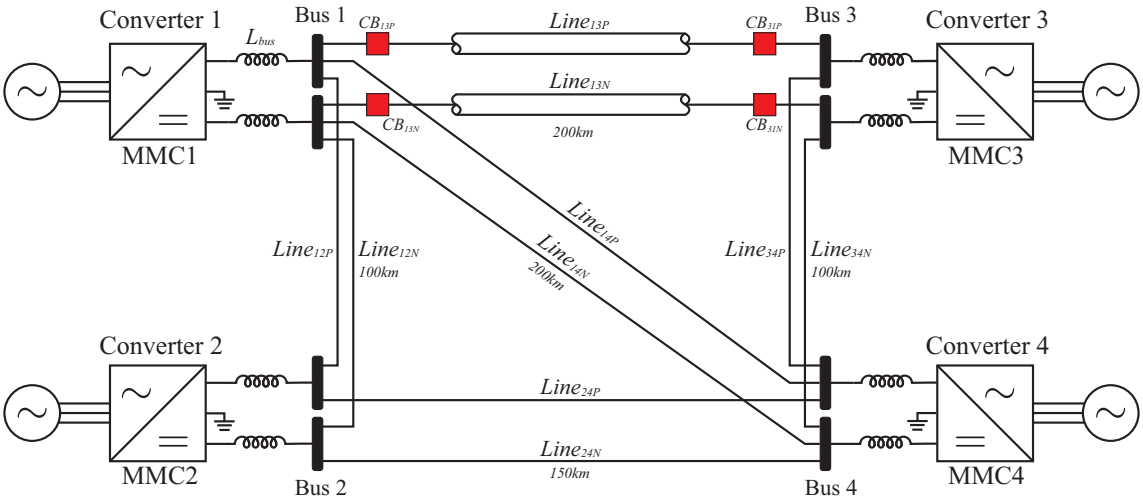

Figure 1.1: Layout of the four-terminal HVDC grid test system [14].

Additionally, both of the aforementioned methods are vulnerable to noise or spikes from measurement instruments such as current and voltage sensors.

In this report, a new backup protection algorithm based on quickest change detection (QCD) method is proposed for MTDC grids. The QCD methods are widely deployed in many fields [10]-[13]. In backup protection settings, the signals from voltage measurements are observed by a decision maker, which monitors any abrupt change in the voltage distribution using sequential measurements. The objective is to detect the change as fast as possible subject to a constraint on the false alarm rate. With sequentially monitoring of signals, the QCD method proposed here is able to quickly trip the breakers under noisy signals with a negligible computation effort. The method is applicable to general N-terminal MTDC grids.

1.2 Test Multi-terminal HVDC System

Fig. 1.1 shows the layout of the test system adopted in this report [14]. The test system, which represents a $\pm$320 kV four-terminal meshed HVDC grid, is comprised of four VSC stations connecting two offshore wind farms to two onshore AC grids. The transmission lines include Line12 and Line34 with 100 km length, Line13 and Line14 with 200 km length, and Line24 with 150 km length. DC breakers are located at both ends of each HVDC link. The detailed configuration of Line13 is depicted in Fig. 1.1 while other lines use simplified representation. Further details of the test system along with its parameters are described in [14].

The DC side of all VSCs are solidly grounded by using DC capacitors at the neutral point. The VSC stations, which are based on the well-known Modular Multilevel Converters (MMCs), are represented by their continuous equivalent models with blocking/de-blocking capabilities [14] [21], as presented in Fig. 1.2(b). The blocking signals of IGBTs are triggered by the converter internal protection shown in Fig. 1.2(c), which consists of overcurrent and undervoltage protection. The

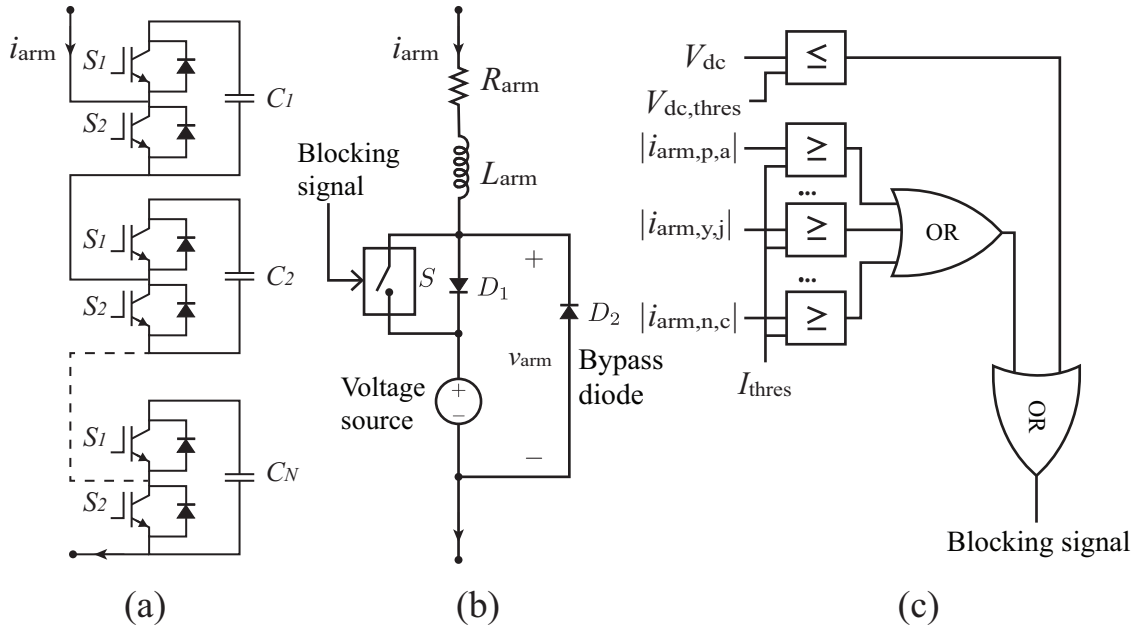

Figure 1.2: Diagrams of MMC models and internal protection. a) submodules (SMs) in a MMC arm; b) continuous equivalent MMC arm model with blacking/de-blocking capabilities [14] [21]; and c) MMC internal overcurrent and undervoltage protection.

arm current threshold is set to be 80% of the maximum instantaneous limit for the IGBT current, while the voltage threshold is selected to be 20% of the nominal DC voltage. The cables are represented by the frequency-dependent model.

The DC circuit breakers (CB_{13P}, etc.) used in the test system of Fig. 1.1 are based on the widely accepted hybrid HVDC circuit breakers [15] with a detailed model presented in Fig. 1.3. The breaker is comprised of parallel connection of an auxiliary branch, which is formed by semiconductor devices in series with a fast mechanical disconnector, and a main branch, which consists of multiple semiconductor devices. The residual breaker is used to isolate the fault to prevent the arrester banks from thermal overload. The proposed backup protection method in this report is general, without any restriction on the configuration of the DC breaker.

1.3 The Proposed Backup Protection Algorithm

In this section, a breaker failure detection algorithm based on the QCD technique for the MTDC grid of Fig. 1.1, is developed and deployed on local DC buses.

1.3.1 Layout of the Protection Unit

The layout of the proposed protection unit is shown in Fig. 1.4. For the sake of simplicity, the positive and negative lines are represented in one line view. As shown in Fig. 1.4, Bus i is con-

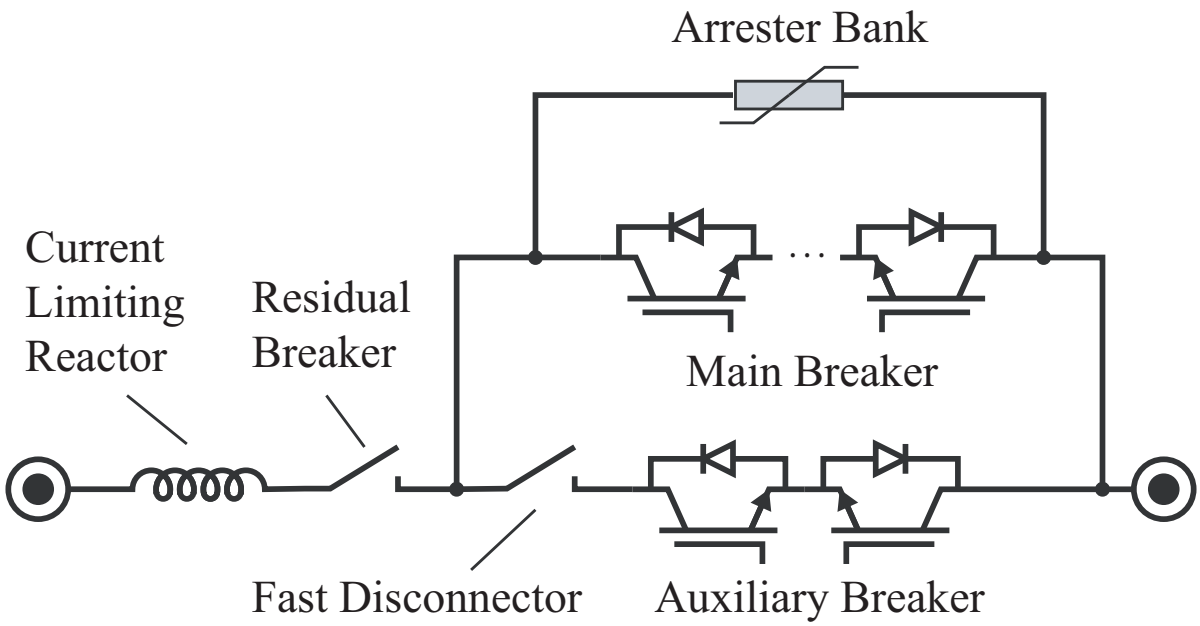

Figure 1.3: Hybrid HVDC circuit breaker adopted in this study.

nected with Converter i through the breaker unit CB_i and with other N buses through breaker units $CB_{i1}, CB_{i2}, ..., CB_{iN}$. These breaker units consist of series connected circuit breakers and sensors that are placed on each circuit breaker and at the end of each HVDC link. The breakers are tripped by signals $T_i, T_{i1}, T_{i2}, ..., T_{iN}$, which are generated by their corresponding relaying algorithm in the primary and backup protection module. The measurements $m_1, m_2, ..., m_N$ consist of voltages across circuit breakers $v^{cbi1}, v^{cbi2}, ..., v^{cbiN}$ and the terminal voltages v^{lij} of those HVDC links which have one of their ends on the local Bus i, where i, j are the two terminals of link ij. These measurements are captured with a sampling frequency f_s and are then directly sent to the data processing unit. They serve as the input to both primary and proposed backup protection algorithms. Subsequent to any fault detection, the backup protection unit waits for the corresponding circuit breaker(s) to trip with the information from available measurements.

1.3.2 The Proposed QCD Algorithm

In case of a DC fault inception, the voltages at bus terminals and across circuit breakers are subject to abrupt changes. These changes occur much faster than the sampling period of the corresponding measurements. The philosophy behind the proposed backup protection algorithm is to determine the operation status of the breakers (breaker failure backup) and primary relay (relay backup) by monitoring any abrupt change in the breaker voltage and the terminal voltage, respectively. A straightforward way to detect such changes would be to compare the target signal with a threshold. However, such an approach would be vulnerable to noise, spikes, or other unexpected errors in the measurements. This problem calls for a detection method with higher robustness. The QCD algorithm [10] is the proposed candidate to this end.

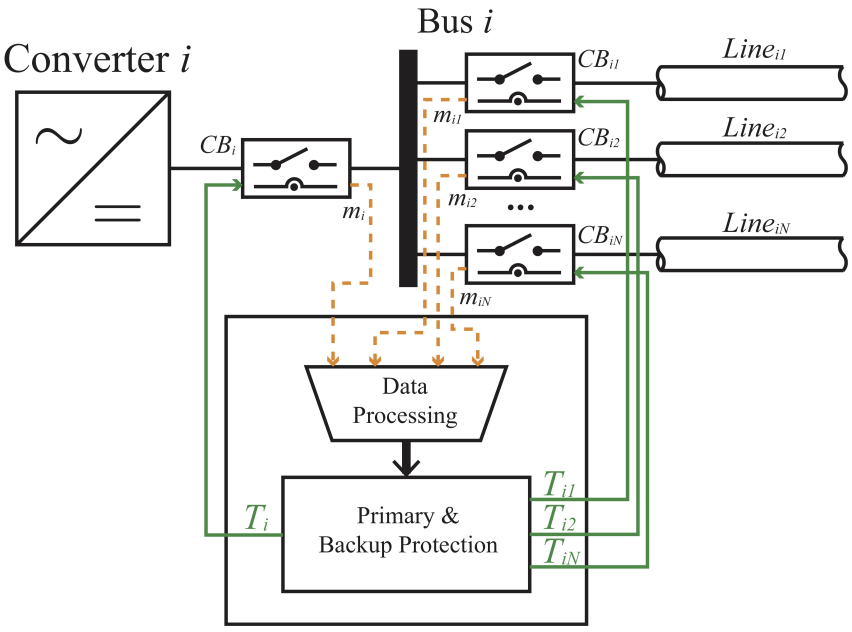

Figure 1.4: The proposed layout of the protection unit at Bus i.

In the context of backup protection, without loss of generality, one can assume that the measurement sequence $m_1, m_2, .., m_k$ is captured by the sensors and sent to the data processing unit. The sequence is an independent Gaussian sequence with a probability density $p_\theta(m)$. The parameter θ denotes the mean of this sequence. Before the unknown change time j, the mean of measurement sequence is θ_0, while after the change time, it becomes $\theta_1 \neq \theta_0$. The goal of the algorithm is to detect this change as fast as possible.

There are two hypotheses to be considered, i.e., $\mathbf{H_0}$ and $\mathbf{H_1}$. $\mathbf{H_0}$ denotes the hypothesis where there are no changes, while $\mathbf{H_1}$ means there is a change in the sequence.

$$\begin{aligned} &\mathbf{H_0} : \theta = \theta_0 \text{ for } 1 \leq i \leq k \\ &\mathbf{H_1} : \text{there exists an unknown } 1 \leq j \leq k \text{ such that} \\ &\quad : \theta = \theta_0 \text{ for } 1 \leq i \leq j-1 \\ &\quad : \theta = \theta_1 \text{ for } j \leq i \leq k \end{aligned} \tag{1.1}$$

The likelihood ratio between hypotheses $\mathbf{H_0}$ and $\mathbf{H_1}$ is

$$\Lambda_1^k(j) = \frac{\prod_{i=1}^{j-1} p_{\theta_0}(m_i) \cdot \prod_{i=j}^{k} p_{\theta_1}(m_i)}{\prod_{i=1}^{k} p_{\theta_0}(m_i)} \tag{1.2}$$

Equation (1.2) expresses the likelihood of measurements to be under $\mathbf{H_1}$ than $\mathbf{H_0}$. The log-likelihood ratio S_j^k is obtained by taking the log of equation (1.2) as

$$S_j^k = \sum_{i=j}^{k} \ln \frac{p_{\theta_1}(m_i)}{p_{\theta_0}(m_i)} \tag{1.3}$$

To detect any unknown change, the maximum likelihood principle is applied on the log-likelihood ratio S_j^k. The decision is made based on the decision function expressed by

$$g_k^m = \max_{1 \le j \le k} S_j^k \tag{1.4}$$

With the aid of (1.4), the alarm time t_a is obtained based on the following rule:

$$t_a = \min\{k : g_k^m \ge h\} = \min\{k : \max_{1 \le j \le k} S_j^k \ge h\} \tag{1.5}$$

where h is a positive threshold chosen based on the system parameters. t_a is the earliest moment when the decision is in favor of $\mathbf{H_1}$ over $\mathbf{H_0}$, i.e., $g_k^m \ge h$.

The calculation of g_k^m could be computationally expensive in digital implementation. Therefore, a new variable g_k, which is a non-negative version of g_k^m, is defined as

$$g_k = \max\{0, g_k^m\} = \max\{0, \max_{1 \le j \le k} S_j^k\} \tag{1.6}$$

g_k^m and g_k are equivalent in the sense that they result in the same alarm time t_a. The proof of this statement is presented in Appendix A.

Based on Appendix B, g_k can be rewritten into the recursive form as

$$g_k = \begin{cases} g_{k-1} + \ln \dfrac{p_{\theta_1}(m_k)}{p_{\theta_0}(m_k)} & \text{if } g_{k-1} + \ln \dfrac{p_{\theta_1}(m_k)}{p_{\theta_0}(m_k)} > 0 \\ 0 & \text{if } g_{k-1} + \ln \dfrac{p_{\theta_1}(m_k)}{p_{\theta_0}(m_k)} \le 0 \end{cases} \tag{1.7}$$

In the settings of the backup protection problem, it is assumed that the distribution of the observation m_i is Gaussian, which is a widely-applied assumption in the literature [20]. Under this assumption, the probability density function with the mean value θ and variance σ^2 is given as

$$p_\theta(m_i) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(m_i-\theta)^2}{2\sigma^2}} \tag{1.8}$$

In this case, the recursive update rule in (1.7) can be rewritten as

$$
\begin{aligned}
g_k &= \max\{0, g_{k-1} + m_k - \frac{\theta_1 + \theta_0}{2}\} \\
&= \max\{0, g_{k-1} + m_k - (\theta_0 + \frac{\nu}{2})\}
\end{aligned}
\tag{1.9}
$$

where $\nu = \theta_1 - \theta_0$ is the minimum possible magnitude of the abrupt change to be detected. Although the Equation (1.9) is derived under Gaussian assumption, the proposed algorithm can be generalized to other distributions as well by plugging their probability density functions into Equation (1.7).

Equation (1.9) corresponds to the well-known cumulative sum (CUSUM) method. The detailed QCD algorithm is shown in Algorithm 1.

Algorithm 1: Backup QCD Algorithm

Input: m_k: measurement sample at step k g: accumulated sum from last step

Output: Decision d

if $k = 0$ **then** /* initialization */

  Read h, θ_0, ν

  $g \leftarrow 0, d \leftarrow False$

end

$g_{next} \leftarrow g + m_k - (\theta_0 + \frac{\nu}{2})$

if $g_{next} > h$ **then** /* change detected */

  $d \leftarrow True$

  $g \leftarrow g_{next}$

else if $g_{next} > 0$ **then** /* update g */

  $g \leftarrow g_{next}$

else /* reset g */

  $g \leftarrow 0$

end

return g, d

Algorithm 1 is executed in real-time with the sampling frequency f_s. m_k denotes the measurement sample taken at each step $k \geq 0$. If there is no signal, k is set to be zero and the algorithm is initialized. g is the data accumulated from the last time step and is updated from the bottom up based on the new inputs. When $m_k > (\theta_0 + \frac{\nu}{2})$, g starts increasing. Once it hits the threshold h, d is set to be *True* and a change is declared.

The proposed method performs the cumulative summation process, which is immune to noise and spikes. In terms of computational effort, within each iteration, at most, three sum, one comparison, and three copy operations are involved in the calculation. Additionally, g, θ_0, ν, and h are the only four variables required to be stored in the memory for the use within each iteration. Based on these facts, the algorithm can be applied easily on most relaying platforms.

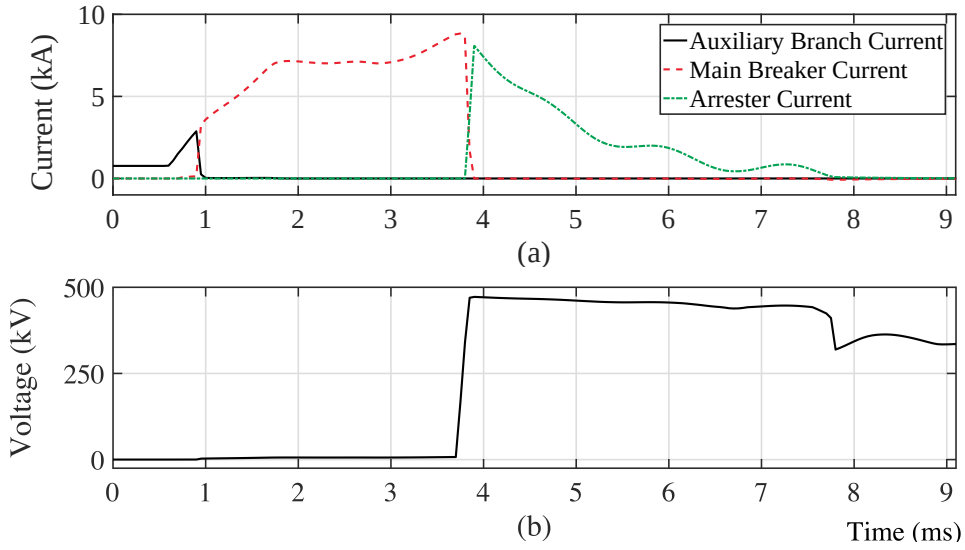

Figure 1.5: Simulated transients of the hybrid circuit breaker CB_{13p} under a pole-to-pole fault in the middle of Line13. a) auxiliary branch, main breaker and arrester currents; and b) voltage across the breaker.

1.3.3 Backup Protection for Breaker Failure

In case of a successful fault detection in primary protection, the fault is sensed and a trip command is sent to the corresponding circuit breakers. *Breaker failure* addresses the scenario where a circuit breaker fails to trip after receiving the tripping signal.

Fig. 1.5 shows the simulated transients of the hybrid circuit breaker CB_{13p} under a pole-to-pole fault in the middle of Line13. After receiving the trip command from the primary relay at $t = 0.9\,\text{ms}$, the fault current starts to be transferred from the auxiliary branch to the main breaker. Once the current commutation is finished, the fast mechanical disconnector opens. Then, starting from $t = 3.8\,\text{ms}$, the current starts decreasing by transferring the fault current to the arrester bank, which establishes a counter voltage across the reactor. The voltage across the breaker, as shown in Fig. 1.5(b), jumps to a high value, which is the summation of this counter voltage and the terminal voltage. The energy accumulated in the reactor and fault current path is then dissipated and the current flowing through the breaker reduces to zero at $t = 7.7\,\text{ms}$. The breaker transients shown in Fig. 1.5 are representing only one of the possible breaker configurations. Since the trip and fault clearance times may vary for different breakers, to verify the validity and applicability of the proposed breaker failure backup algorithm to different breaker configurations, simulation results are provided in Section IV.B.

In the DC circuit breaker design, to diminish the fault current, the voltage rating of the arrester bank must be larger than the DC voltage. After commutating the current to the arrester bank, the voltage across the breaker rises shapely from zero to a value which exceeds the nominal DC voltage. This counter voltage is a clear sign that the circuit breaker works properly and starts to

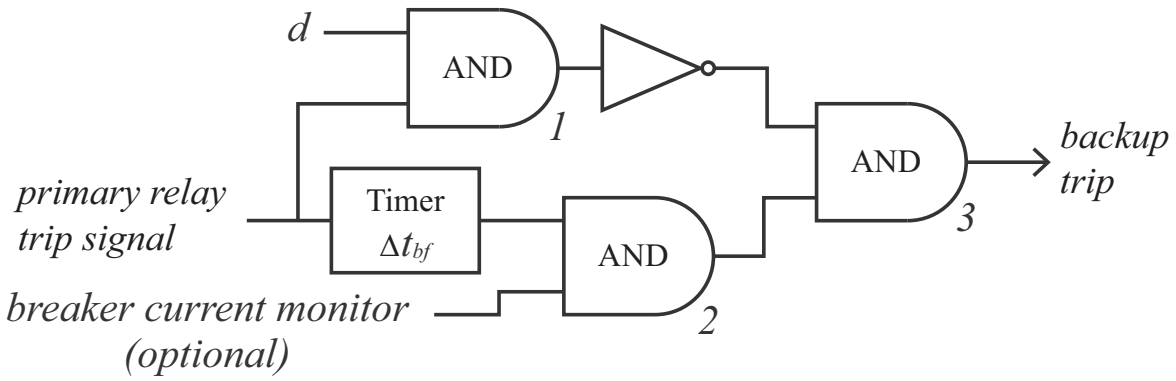

Figure 1.6: Breaker failure backup protection scheme.

interrupt the fault current as expected. Therefore, the problem of detecting breaker failure can be reduced to detecting an abrupt change in the sequence of the breaker voltage.

The proposed QCD method is applied here to detect the change in this case. Measurements $m_{k,k\geq 0}$ are voltage samples $v_{k\ ,k\geq 0}^{cb}$ across the breaker. The overall scheme of the breaker failure backup protection is presented in Fig. 1.6. After receiving the trip signal from the primary relay at time instant t_d, AND gate 1 is activated and the QCD decision variable d is closely monitored. If an abrupt change is detected, a successful breaker operation is observed and d is set to be 1. In this case, AND gate 3 is deactivated and the backup protection will not trip. Meanwhile, at $t = t_d$, a timer is initialized with a delay of breaker normal clearing time Δt_{bf} (4 ms in this study). For additional security, the currents flowing through the breakers can be monitored as optional measurements. If the current is higher than twice the nominal current when the timer times out (exceeding Δt_{bf}), AND gate 2 will be satisfied. If d is 0 at this instant, it is concluded that the breaker has failed and the backup trip signals will be sent to the adjacent breakers located on the same bus. These breakers will take over and clear the fault.

1.3.4 Backup Protection for Relay Failure

Backup protection of breaker failure is based on the fact that the DC fault is detected correctly by the primary protection. However, due to failure of primary relying algorithm or communication system, there is a chance that the primary relay fails to detect the fault. In this case, it is crucial to equip the system with a backup protection scheme for relay failure as well.

Generally, during any pole-to-pole or low-impedance pole-to-ground faults in an MTDC grid, the fault current increases sharply and the system dynamics responses in three stages. The first stage is a natural response of the DC link capacitors close to each terminal. During this stage the IGBTs are not blocked yet. In the second stage, the IGBTs are blocked and the fault current starts commutating to the converter freewheeling diodes. The third is the grid-side current feeding stage, in which the grid current contributes to the fault.

Effective design of primary and backup relaying algorithms ensures a detection of fault within 2 ms, which is in the first stage. Provoked by the fault, travelling waves propagate on the faulty link and reflect at either the fault location or a bus terminal. When the step-shaped wave arrives to the bus terminal, a rapid change in bus voltage is observed. This change is a critical alert for detection of a fault. Therefore, the backup protection of relay failure can be reduced to detection of an abrupt change in the probability distribution of the sequence of link voltages at each terminal. Similarly, the proposed QCD algorithm is implemented to identify this change. In this case, measurement samples $m_{k,k\geq 0}$ are $v_k^{lij}{}_{,k\geq 0}$. The relay failure backup algorithm works in cooperation with each primary relay. When a fault is detected by the QCD algorithm for relay failure, it will check if there exists a trip signal from the primary relay. If not, the backup algorithm will wait for Δt_{rf} (3 ms in this study) and trip the corresponding breaker after this delay.

1.3.5 Overall Protection Scheme

With the setup of backup protection scheme for both breaker and relay failures, the overall protection scheme is summarized here. Within each time step Δt, the status of the system is continuously monitored by both the primary and proposed QCD algorithm for relay backup. In case a fault is detected, the QCD algorithm for breaker failure is triggered. If the breaker is tripped successfully, no more action is required and the algorithm moves to the next step. If the fault is not cleared, an alert will be sent and the backup protection will take an action to trip other breakers on the same bus.

1.4 Simulation Results

In this section, a set of simulation results are presented to evaluate performance and effectiveness of the proposed backup protection algorithm under five scenarios: a) a pole-to-pole fault under normal operation conditions; b) a low-impedance pole-to-ground fault; c) a high-impedance pole-to-ground fault d) reversed power flow; and e) presence of noise and spike. The test system of Fig. 1.1 is implemented in the PSCAD/EMTDC software environment. A sampling frequency of $f_s = 50\,\text{kHz}$ is adopted in all simulations. The measurements in these simulations are not specifically assumed to be Gaussian distributed. For the sake of simplicity, the fault injection time is normalized to $t = 0\,\text{ms}$ in the following figures.

1.4.1 Base Case

This is the reference case where 800 MW and 600 MW are distributed to Converters 3 and 4, respectively, from Converters 1 and 2, which both input 700 MW to the MTDC grid. In this scenario, the system of Fig. 1.1 is subjected to a pole-to-pole fault located on the middle of Line13.

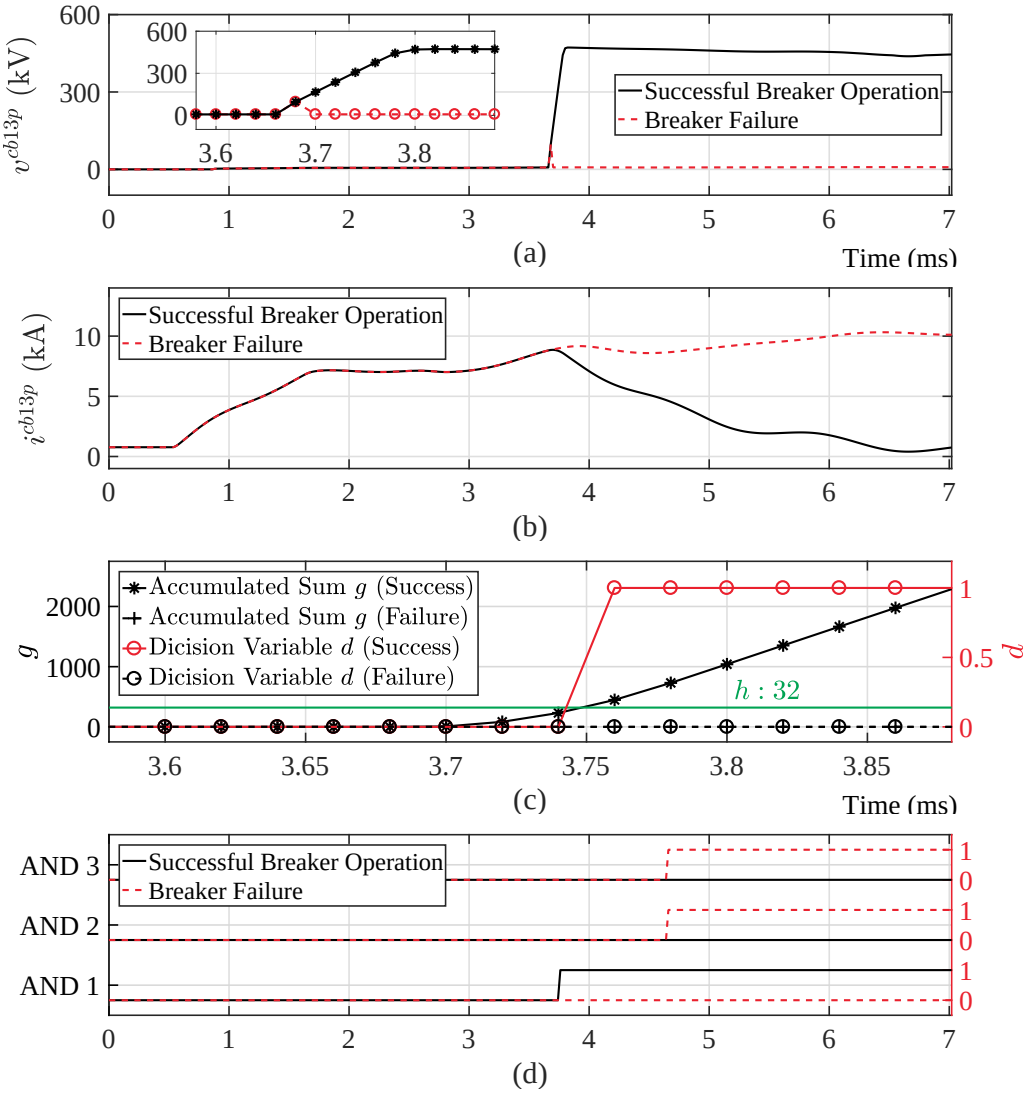

Figure 1.7: Simulation results with a pole-to-pole fault in the middle of Line13, under both successful breaker operation and breaker failure: (a) voltage across circuit breaker v_{cb13p}, (b) current flowing through circuit breaker i_{cb13p}, (c) zoomed-in portion of outputs from beaker failure QCD algorithm, and (d) outputs of AND gates 1, 2, and 3 from Fig. 1.6.

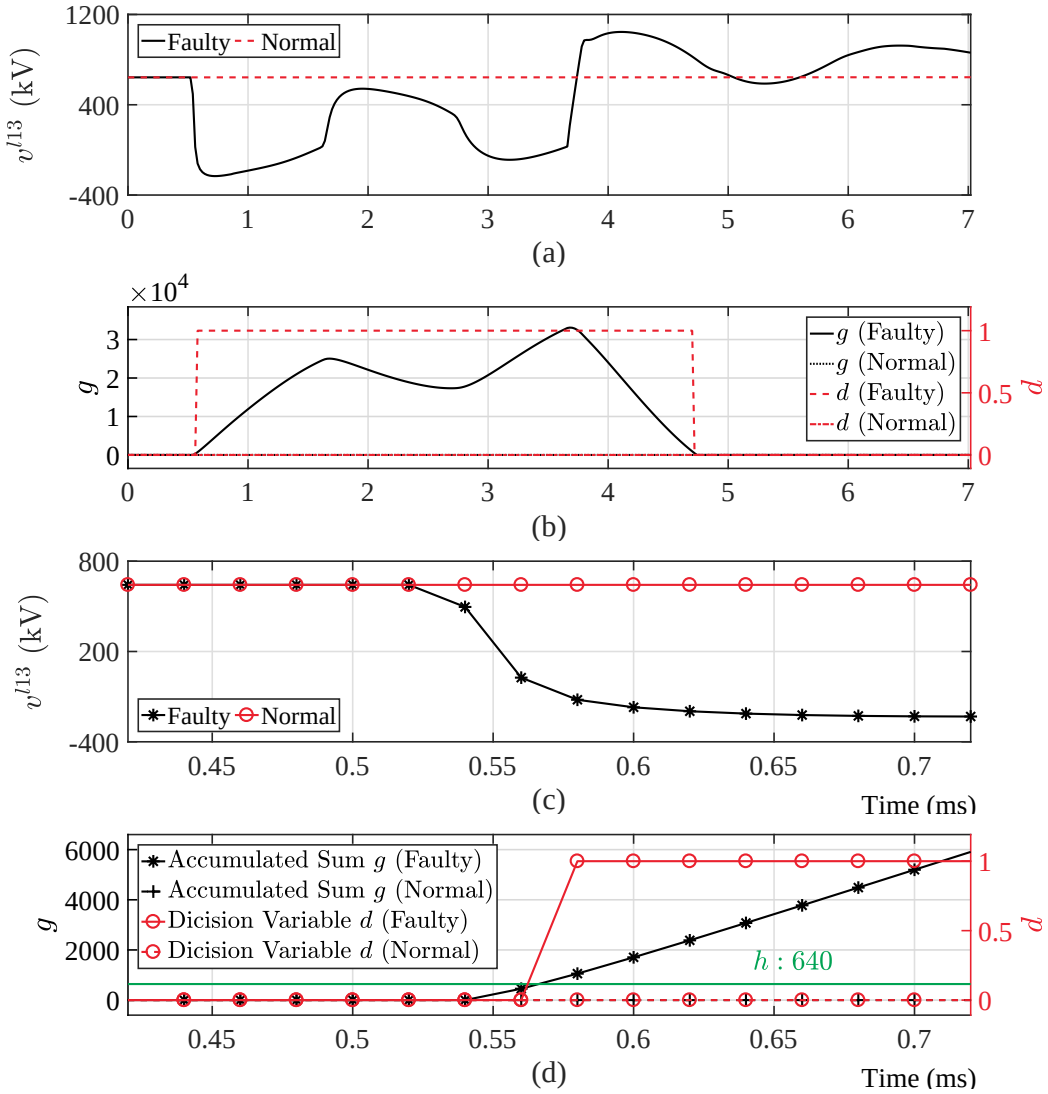

Figure 1.8: Simulation results with a pole-to-pole fault in the middle of Line13, under both normal and faulty conditions: (a) v^{l13}, voltage of Line13 at Bus 1, (b) outputs from beaker relay backup algorithm, (c) and (d) zoomed-in portion of (a) and (b), respectively.

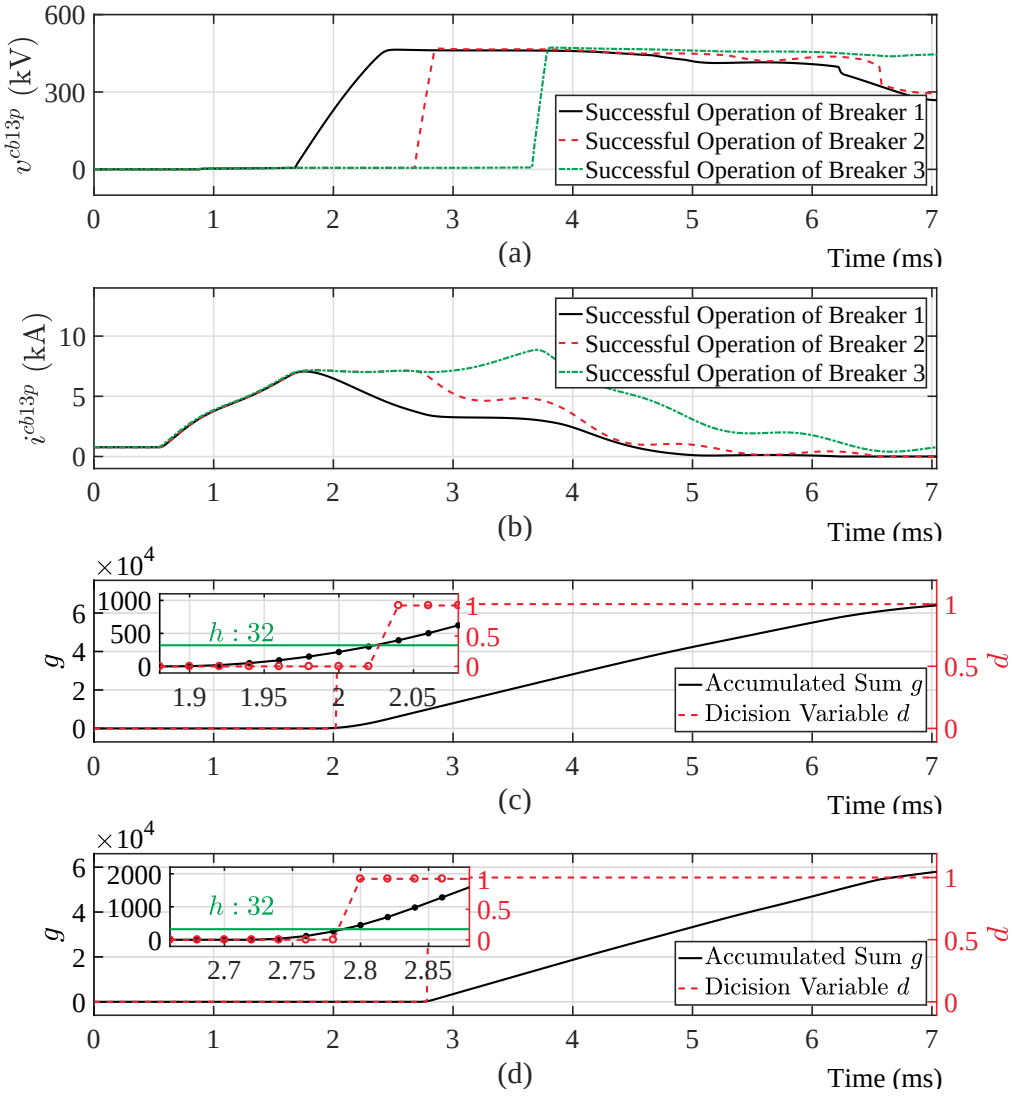

Figure 1.9: Simulation results with different breaker configurations: (a) voltage across the circuit breaker v_{cb13p}, (b) current flowing through the circuit breaker i_{cb13p}, (c) outputs of the beaker failure QCD algorithm under successful breaker operation for breaker 1, (d) outputs of the beaker failure QCD algorithm under successful breaker operation for breaker 2.

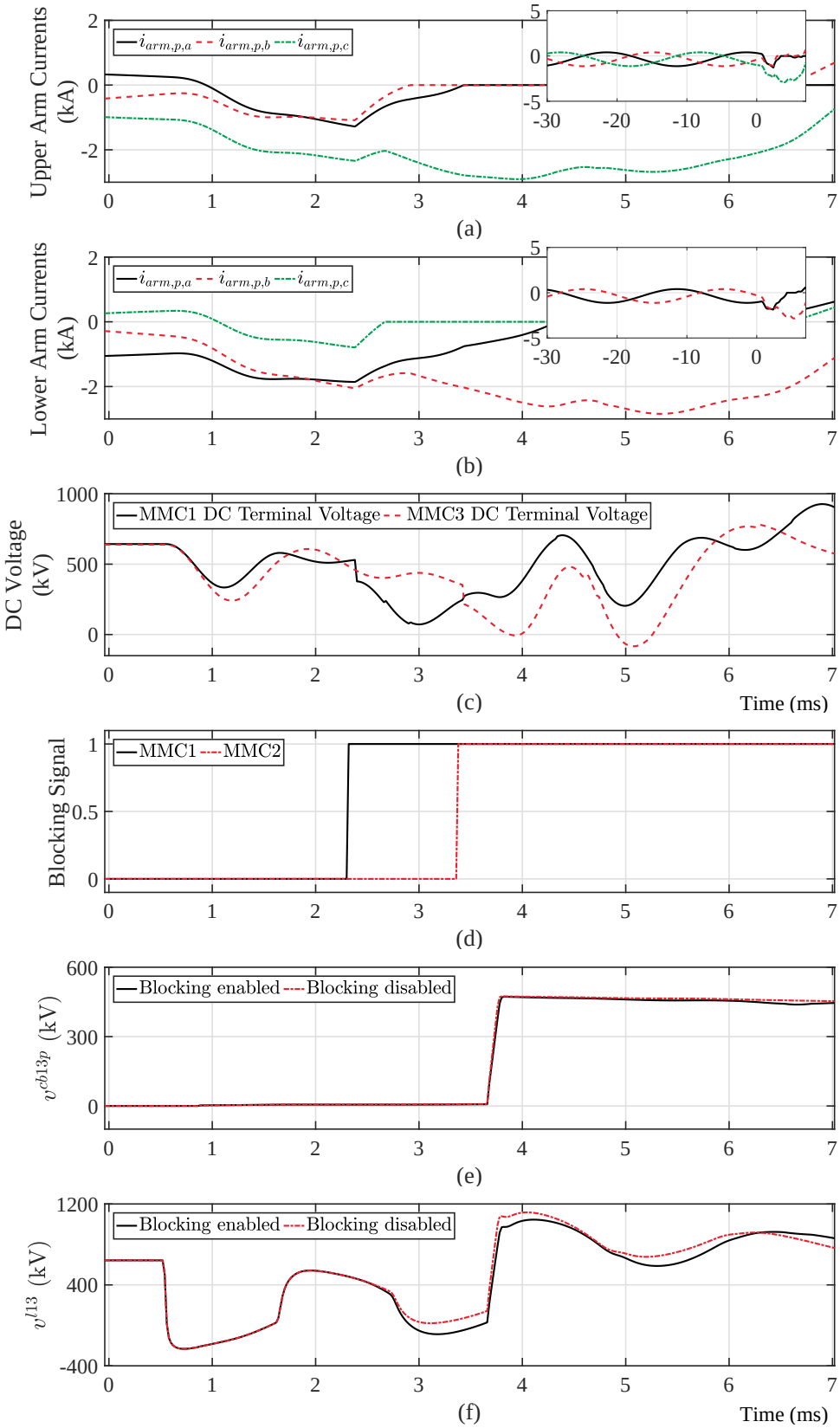

Figure 1.10: Simulation results of converter internal protection quantities with a pole-to-pole fault in the middle of Line13: (a) upper arm currents of MMC1, (b) lower arm currents of MMC1, (c) DC voltage on MMC1 terminal side and MMC3 terminal side (for undervoltage internal protection), (d) blocking signals of MMC1 and MMC2, (e) voltage across the circuit breaker v_{cb13p} with and without converter blocking enabled, and (f) v^{l13}, voltage of Line13 at Bus 1 with and without converter blocking enabled.

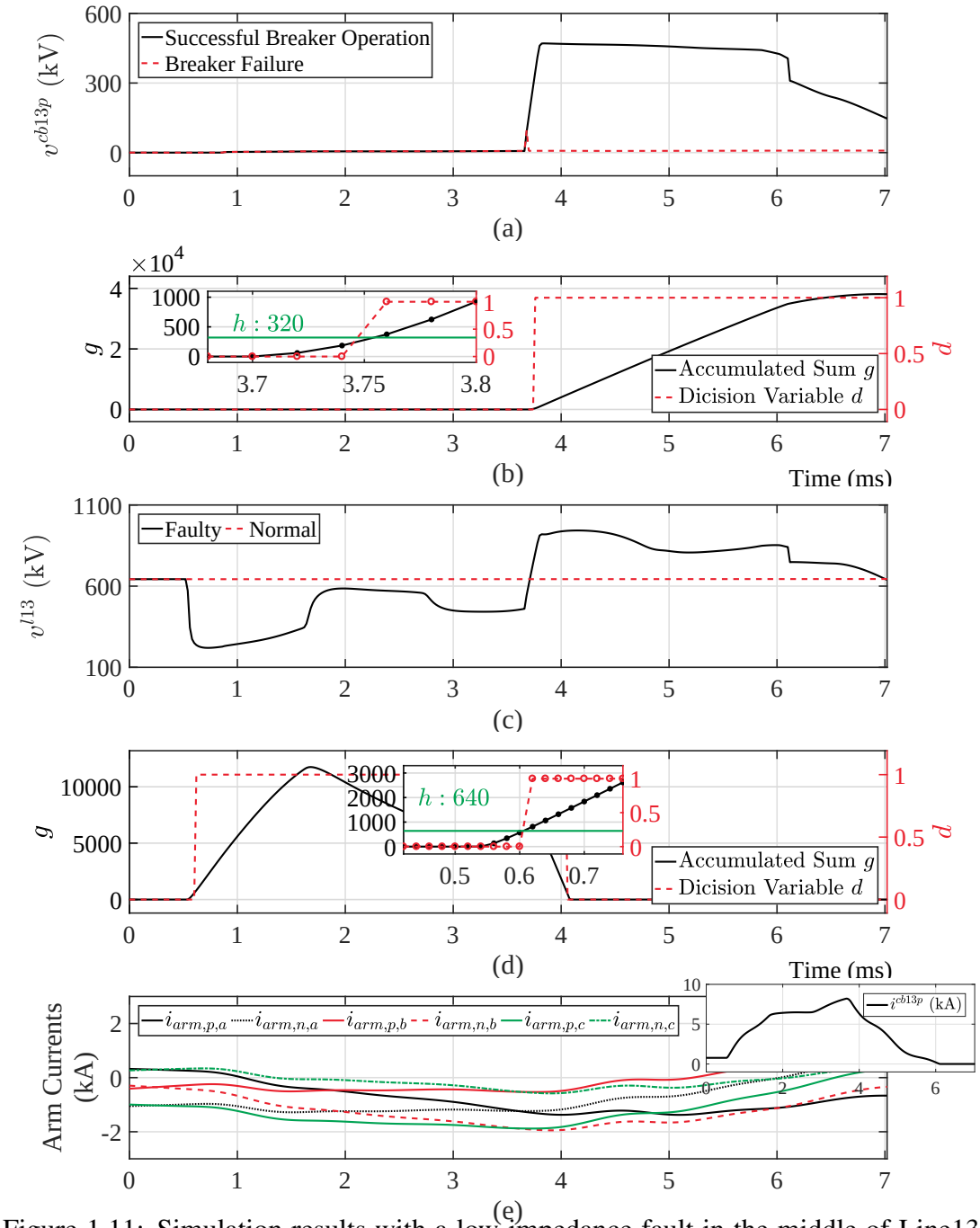

Figure 1.11: Simulation results with a low-impedance fault in the middle of Line13: (a) voltage across the circuit breaker v_{cb13p}, (b) outputs of the beaker failure QCD algorithm under successful breaker operation, (c) v^{l13}, voltage of Line13 at Bus 1, (d) outputs of the relay failure backup algorithm during the fault, and (e) arm currents of MMC1, and positive pole current of Line13 i^{l13p}.

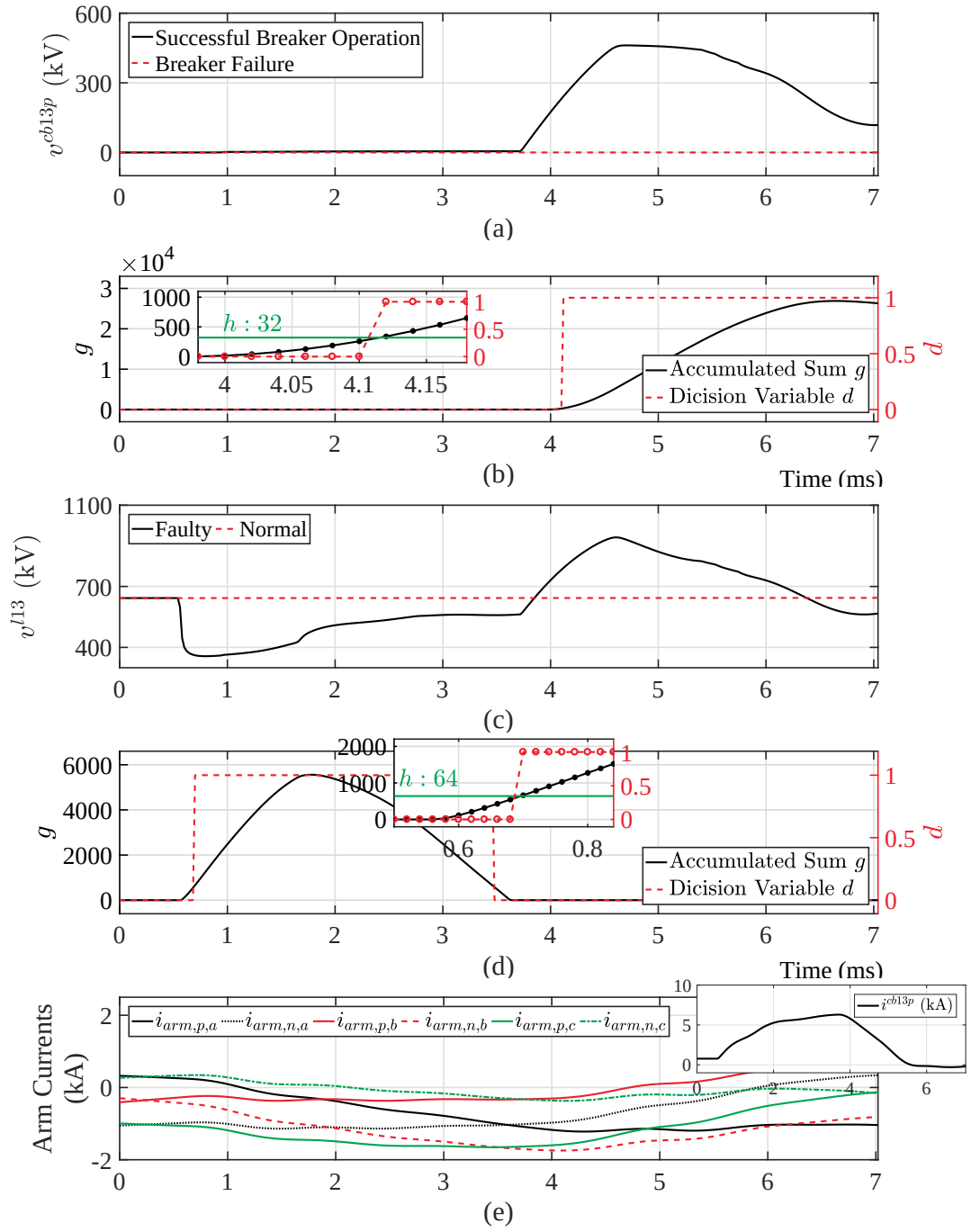

Figure 1.12: Simulation results with a high-impedance fault in the middle of Line13: (a) voltage across the circuit breaker v_{cb13p}, (b) outputs of the beaker failure QCD algorithm under successful breaker operation, (c) v^{l13}, voltage of Line13 at Bus 1, (d) outputs of the relay failure backup algorithm during the fault, and (e) arm currents of MMC1, and positive pole current of Line13 i^{l13p}.

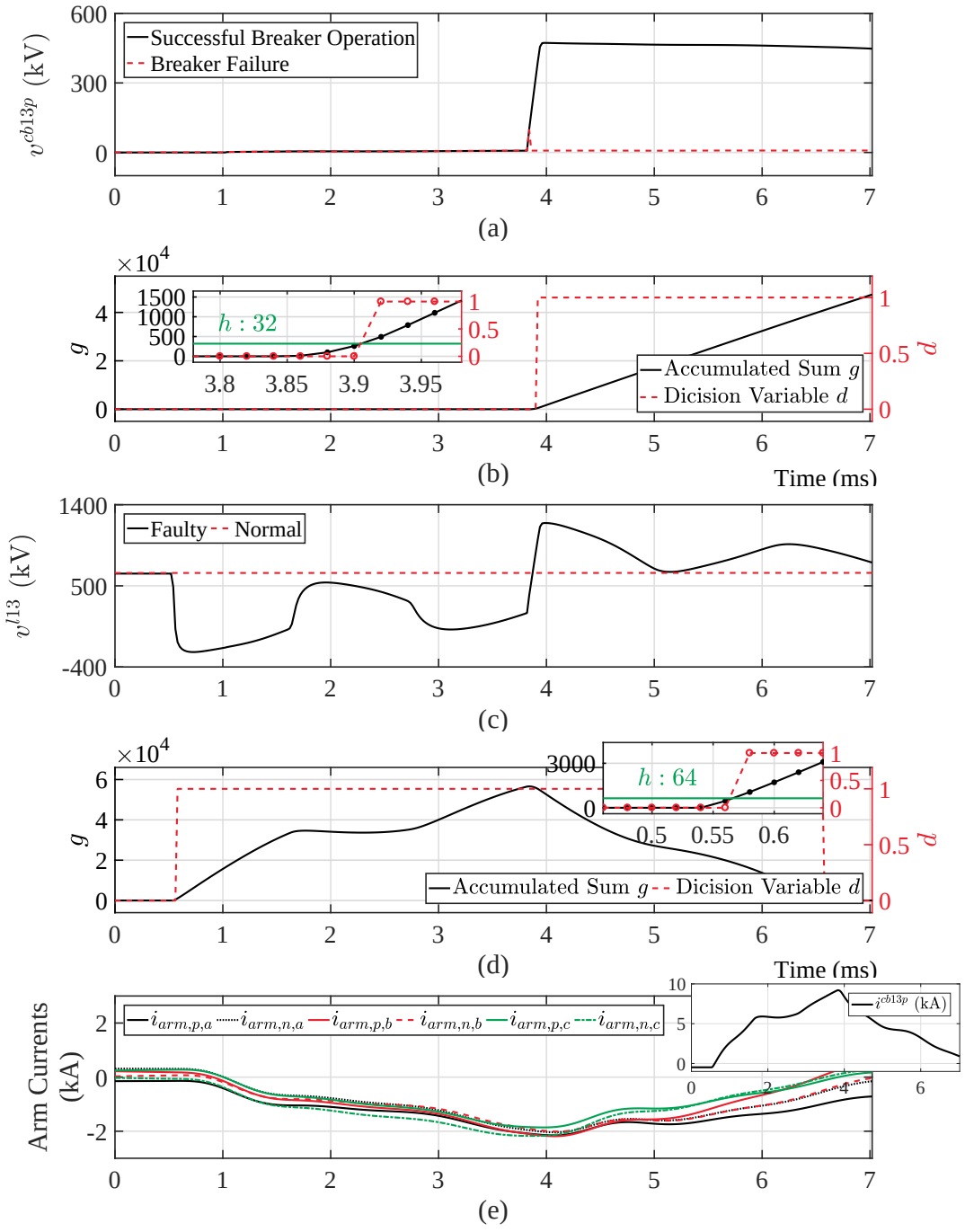

Figure 1.13: Simulation results under reversed power flow: (a) voltage across the circuit breaker v_{cb13p}, (b) outputs of the beaker failure QCD algorithm under successful breaker operation, (c) v^{l13}, voltage of Line13 at Bus 1, (d) outputs of the relay failure backup algorithm during the fault, and (e) arm currents of MMC1, and positive pole current of Line13 i^{l13p}.

The simulation results are demonstrated in Fig. 1.7. As described in Section III, the voltage across the circuit breaker (CB_{13P} in this case) is used for breaker failure detection. v^{cb13p} with both proper breaker operation and breaker failure are depicted in Fig. 1.7(a). Under the breaker failure condition, v^{cb13p} remains close to zero while the signal jumps to a high value in the case where the fault is successfully cleared. In the proposed algorithm, the accumulated sum g and the decision variable d are updated within every step in Algorithm 1. A zoomed-in view of g and d is presented in Fig. 1.7(c). When the breaker works properly, v^{cb13p} starts to increase at $t = 3.66$ ms, which means that the fault current is being commutated from the main breaker branch to the arresters. g keeps accumulating because of the high value of signal v^{cb13p}. At $t = 3.76$ ms, g becomes higher than the threshold h (marked as the horizontal line), resulting in the change of d from 0 to 1. This change indicates that the breaker operates normally. In this case, AND gate 1 is satisfied and outputs 1, as shown in Fig. 1.7(d). The condition 1 from AND gate 1 deactivates AND gate 3, preventing a backup trip. However, if the breaker fails to operate properly, g and d remain zero, which result in a zero output from AND gate 1. Then, the state of AND gate 3 is dominated by the state of AND gate 2, which is determined by two conditions, i.e., the delayed trip signal from the primary relay and the presence of uncleared current flow. After a time delay of Δt_{bf}, the primary relay trip signal is sent to AND gate 2 at $t = 4.68$ ms. As shown in Fig. 1.7(b), the current (i^{cb13p}) flowing though breaker is higher than twice the nominal current. Therefore, the outputs of both AND gate 2 and 3 switch to 1, indicating a breaker failure condition.

It is noteworthy that the threshold h and minimum detectable magnitude ν in Algorithm 1 are simply selected to be 320 kV, which is the nominal voltage of the HVDC system. The pre-fault mean, θ_0, is zero here. h, ν and θ_0 are kept unchanged for all the following breaker failure protection scenarios.

Similarly, the results of the relay backup protection algorithm is provided in Fig. 1.8. v^{l13}, the pole-to-pole voltage of Line13 at Bus 1 is the measurement being monitored (Fig. 1.8(a)). To adopt the same algorithm as the breaker failure detection, $-v^{l13}$ is fed into Algorithm 1. When the wavefront arrives at the terminal of Bus 1 during a fault, v^{l13} drops quickly, which results in an increase in g (Fig. 1.8(b)). At $t = 0.58$ ms, d changes to 1, indicating a fault detection. On the contrary, both g and d remain zero under normal conditions. As described in Section III, the relay failure protection will trip if the primary relay does not detect the fault prior to $t = 3.58$ ms, which is the summation of 0.58 ms, the detection time and 3 ms, the delay Δt_{rf}. The zoomed-in views of Figs. 1.8(a) and (b) are presented in Figs. 1.8(c) and (d), respectively. h and ν are set to be 640 kV and 320 kV, which are the nominal values of the pole-to-pole and pole-to-ground voltage of the DC links, respectively. $\theta_0 = -640$ kV is adopted in Algorithm 1. These values of h, ν and θ_0 are used for all the following relaying failure protection scenarios.

Proper selection of the threshold values ensures that the abrupt changes are precisely detected while keeping a low false alarm rate. The values selected in this study, i.e., 320 kV and 640 kV, can be easily obtained from the system parameters. These thresholds keep a balance between the detection speed and false alerts.

1.4.2 Compatibility with Different Breaker Configuration

In this section, two more breakers, i.e., breakers 1 and 2, are implemented to test the compatibility of proposed backup algorithm with different breaker configurations. These two new breakers have different delays and fault clearance times, as depicted in Fig. 1.9(a). Breaker 3 is the same breaker used in the base case and is presented here as a reference. The currents flowing through these breakers are shown in Fig. 1.9(b). As shown in Fig. 1.9, with different breakers deployed, the fault is cleared with different speeds. The outputs from the QCD algorithm applied to breakers 1 and 2 are shown in Figs. 1.9(c) and (d), respectively. These results verify that the proposed backup algorithm is equally applicable to different breaker configurations.

1.4.3 Blocking of IGBTs

Subsequent to a fault on any DC link, the MMC arm currents exceed their rating values. Once the arm currents exceed a threshold value, the desaturation detection of IGBTs will act, thereby blocking them to avoid any thermal overload. The converter is also blocked under low DC voltage due to the loss of controllability. The implemented scheme is presented in Fig. 1.2(c). A pole-to-pole fault in the middle of Line13 is imposed on the test system at $t = 0.71$ s. The six arm currents of MMC1 are plotted in Figs. 1.10(a) and (b). The current threshold I_{thres} is set to be 2.31 kA based on the rating of MMC1, i.e., 80% of the maximum instantaneous arm current, which is 2.88 kA. Subsequent to the fault occurrence, MMC1 and MMC2 are blocked after 2.3 ms and 3.4 ms, respectively. In this case, as shown in Fig. 1.10(c), the DC voltage on MMC1 terminal drops below 20% of the DC nominal voltage after the blocking of MMC1. The converter will not be re-blocked by the undervoltage protection. The voltage across breaker v^{cb13p} (used for breaker failure backup) and the voltage of Line13 v^{l13} (whose first wave is used for relay failure backup) are presented in Figs. 1.10(e) and (f), respectively. These voltages are measured with and without converter blocking enabled. The waveforms of Figs. 1.10(e) and (f) highlight that the sequence of converter blocking/de-blocking does not interfere with the operation and performance of the proposed backup protection algorithms, which rely on the voltage across the breaker and the first wave of line side DC voltage. Therefore, the functionalities of the breaker and relay failure backup protection algorithms are not affected.

1.4.4 Low-Impedance Pole-to-ground Fault

In this scenario, the system is subjected to a low-impedance pole-to-ground fault on the positive pole of Line13 (100 km from Bus 1). The fault impedance is 0.5 Ω. The results from the backup protection for both breaker (Figs. 1.11(a) and (b)) and relay failure (Figs. 1.11(c) and (d)) are provided. The QCD algorithm outputs under breaker failure and normal conditions are all zero and not presented. As shown in Fig. 1.11(e), none of the arm currents exceed I_{thres}. As the result, MMC1 is not blocked in the first 7 ms.

In this case, v^{cb13p} presents a similar behavior to the reference scenario. Fig. 1.11(b) confirms the detection of successful fault clearance at $t = 3.76$ ms, when d changes from zero to one. The

voltage drop of v^{l13} (Fig. 1.11(c)) is not as large as the change in the reference case (Fig. 1.8(a)) and, therefore, it results in a slower accumulation of g. However, the relay failure backup algorithm still works well and detects the fault at $t = 0.62\,\text{ms}$.

1.4.5 High-Impedance Pole-to-ground Fault

In this scenario, a high-impedance pole-to-ground fault is imposed on the positive pole of Line13 (100 km from Bus 1). A $10\,\Omega$ fault impedance is inserted between the fault location and the ground. With a higher fault impedance applied, the drop of voltage magnitude is even smaller compared to the low-impedance case. However, as shown in Fig. 1.12, both breaker failure backup and relay backup protection algorithms response well.

1.4.6 Reversed Power Flow

In this scenario, the system is tested under the same fault in the reference case. The difference lies in the direction and distribution of power flow. In this case, Converters 3 and 4 both export 500 MW to the MTDC grid while Converters 1 and 2 transfer 200 MW and 800 MW, respectively, to the AC grid. The results presented in Fig. 1.13 demonstrate satisfactory performance of the proposed algorithm.

1.4.7 Comparison with the Existing Methods

In this section, the results from the proposed backup protection method are compared with the classifier based backup method [7] [8]. To this end, both the signals, v^{cb13p} and v^{l13}, are contaminated by adding noise and spikes. These signals are processed by the proposed and existing algorithms. The corresponding results are shown in Figs. 1.14 and 1.15.

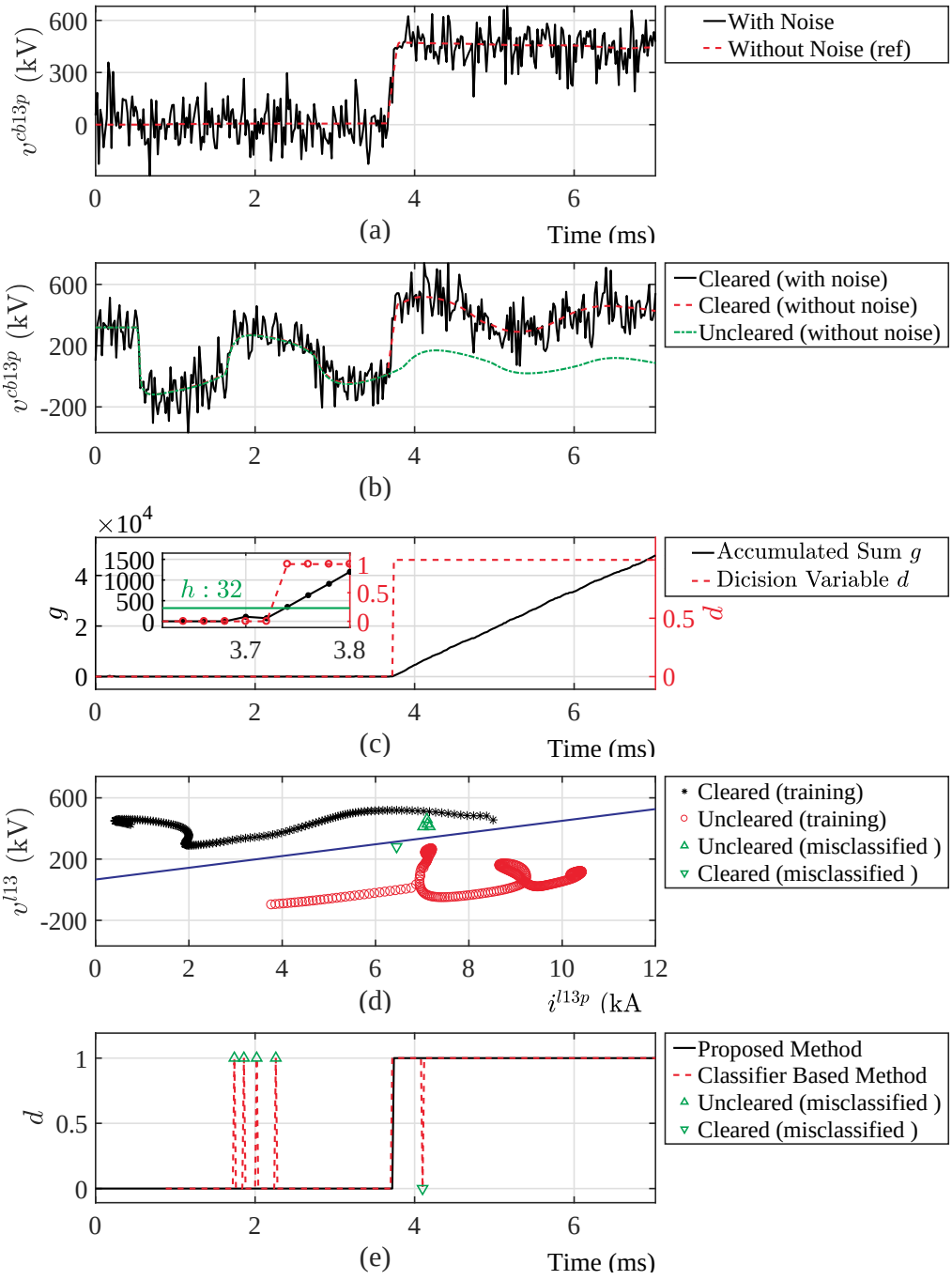

Figure 1.14: Comparison under noise. (a) voltage across the circuit breaker v_{cb13p}, (b) v^{l13}, voltage of Line13 at Bus 1, (c) and (d) results from the proposed and classifier-based methods, and (e) decision variables.

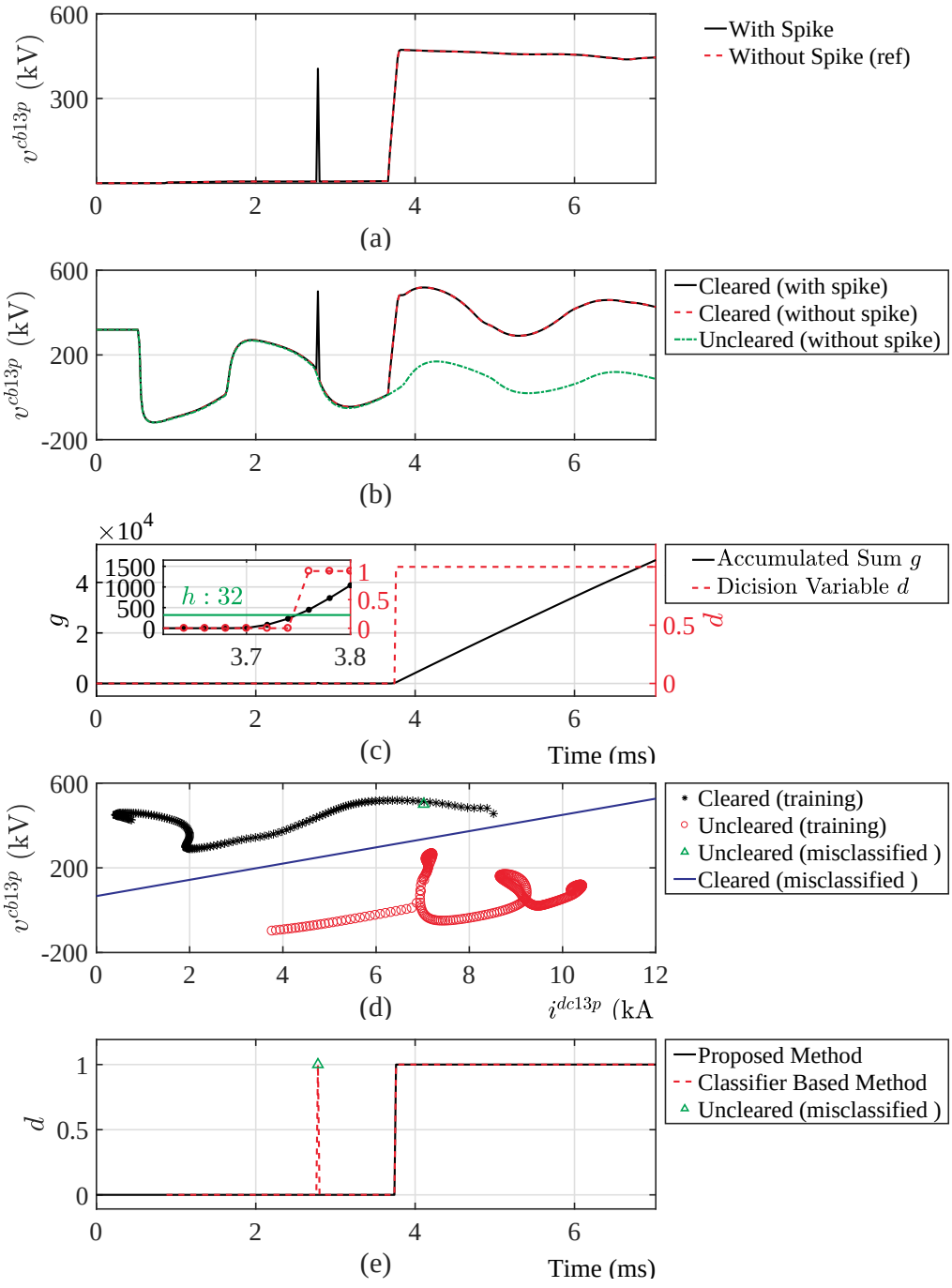

Figure 1.15: Comparison under spike. (a) voltage across the circuit breaker v^{cb13p}, (b) v^{l13}, voltage of Line13 at Bus 1, (c) and (d) results from the proposed and classifier-based method, and (e) decision variables.

To test the impact of noise, an independent and identically distributed sequence drawn from a Gaussian distribution $\mathcal{N}(0,100)$ is applied and added to the original signals as shown in Figs. 1.14(a) and (b). Unlike the classifier based method, the accumulated sum g, which is shown in Fig. 1.14(c), is not affected by the presence of such noise. Fig. 1.14(d) shows the scatter plot (UI characteristic) of voltage, v^{l13} and current, i^{l13p} used for the classifier based algorithms. The space is separated by a decision boundary (marked in purple line). A fault is said to be cleared if the instantaneous measurement lies in the upper space while it is declared as uncleared when it appears in the lower space. In the presence of noise, some of the samples which should lie in the "uncleared" portion are misclassified into the upper space (marked in upward-pointing triangles). Similarly, some "cleared" samples are misclassified into the lower space (marked in downward-pointing triangles). In Fig. 1.14(e), the decision variables from the proposed and classifier-based algorithm are compared. Before the actual starting time of fault clearance at $t = 3.66\,\text{ms}$, the classifier based algorithm declares detection of successful breaker actions ($d = 1$) at around $t = 2\,\text{ms}$ (upward-pointing triangles). Additionally, after $t = 3.66\,\text{ms}$, some of the samples (downward-pointing triangles) are classified as "uncleared" again. These misclassifications result in false trip signals.

Fig. 1.15 shows the performances of the proposed and classifier based algorithms under the effect of a 400 kV spike at $t = 2.8\,\text{ms}$. The spike introduces an abnormally high voltage prior to fault clearance, resulting in a misclassification of an "uncleared" sample into a "cleared" one by the classifier-based method. As confirmed in Fig. 1.14, performance of the proposed algorithm is not degraded under this case as well.

With respect to the computational burden, there are two additional drawbacks by using the classifier-based method:

- A K nearest neighbor (KNN) classifier, which is used as an example in [8], has to be trained with data from different types of faults under various scenarios. For example, for a pole-to-pole fault, the fault characteristic varies with the faulty link, fault location and fault impedance. The classifier has to be trained with data from all possible cases. The proposed method uses the same framework for all scenarios, with a much more simplified procedure.
- To make a correct decision based on the KNN, all historical current and voltage data has to be stored in the relay, thereby demanding a huge amount of data storage. Compared to the classifier-based method, the proposed method only keeps record of the cumulative sum and other three variables, which are fixed sized floating numbers and take a negligible space.

1.5 Conclusion

In this report, a local measurement-based backup protection algorithm for MTDC grids is proposed. The proposed algorithm that is based on the quickest change detection (QCD) technique, achieves fast and accurate backup protection functionality for the primary relay to ensure a higher reliability in the system. The proposed method can be readily extended to different grid configurations and is able to cooperate with different primary protection algorithms and breaker configu-

rations. Performance and effectiveness of the proposed algorithm are evaluated and verified based on time-domain simulation studies in the PSCAD/EMTDC environment. The results confirm satisfactory performance of the proposed algorithm in terms of accuracy, robustness, and speed under various fault scenarios.

A. Proof of the Equivalence of g_k and g_k^m

The variables g_k^m and g_k are defined as

$$g_k^m = \max_{1\le j\le k} S_j^k \tag{.1}$$

$$g_k = \max\{0, g_k^m\} = \max\{0, \max_{1\le j\le k} S_j^k\} \tag{.2}$$

First, it is to be proved that when an alarm is triggered using g_k^m, an alarm is also triggered using g_k at the same time. Given the alarm time

$$t_a = \min\{k : g_k^m \ge h\} = \min\{k : \max_{1\le j\le k} S_j^k \ge h\} \tag{.3}$$

where h is a positive threshold.

Equivalently, the following statements hold:

$$\begin{aligned} &0 < h \le g_{t_a}^m, \\ &g_k^m < h, k \in \{0,1,...,t_a-1\} \end{aligned} \tag{.4}$$

Therefore, based on the definition of g_k, it is deduced that

$$\begin{aligned} g_k &= \max\{0, g_k^m\} \\ &= \begin{cases} g_{t_a}^m \ge h, \text{if } k = t_a \\ g_k^m < h, \text{if } 0 < g_k^m < h, k \in \{0,1,...,t_a-1\} \\ 0 < h, \text{if } g_k^m \le 0, k \in \{0,1,...,t_a-1\} \end{cases} \end{aligned} \tag{.5}$$

which means that g_k sets the same alarm time as g_k^m. Next, it is to be proved that whenever g_k triggers an alarm at t_a, g_k^m triggers one as well. This condition can be expressed as

$$\begin{aligned} &0 < h \le g_{t_a}, \\ &0 \le g_k < h, k \in \{0,1,...,t_a-1\} \end{aligned} \tag{.6}$$

Thus, the value of g_k^m is

$$\begin{aligned} &0 < h \le g_{t_a} = g_{t_a}^m, \\ &g_k^m \le g_k < h, k \in \{0,1,...,t_a-1\} \end{aligned} \tag{.7}$$

which means that g_k^m sets an alarm at t_a as well.

B. Derivation of The Recursive Form of g_k

Considering the non-negative definition of g_k in (1.6), at every time step k, there are two cases, i.e., $g_{k-1} = 0$ and $g_{k-1} > 0$. $g_{k-1} = 0$ implies that the maximum summation of log-likelihood ratio from a certain time step j to the last time step $k-1$ is either negative or zero. Thus, the newly calculated log-likelihood ratio at current step determines the value of g_k. This condition can be expressed as

$$g_k = \max\{0, \ln \frac{p_{\theta_1}(m_k)}{p_{\theta_0}(m_k)}\} \tag{.1}$$

If $g_{k-1} > 0$, the maximum summation at step k can be calculated by summing two parts, i.e., the newly calculated log-likelihood ratio at current step k and the maximum value from last step $k-1$. This relationship can be written as

$$g_k = \max\{0, g_{k-1} + \ln \frac{p_{\theta_1}(m_k)}{p_{\theta_0}(m_k)}\} \tag{.2}$$

Equations (.1) and (.2) can be merged into one expression, which is the recursive form of g_k provided in (1.7).

2. Reducing the Fault Transient Magnitudes in Multi-terminal HVDC Grids by Sequential Tripping of Hybrid Circuit Breaker Modules

2.1 Introduction

The global need for reliable and efficient energy supplies and the necessary shift from fossil fuels to renewable energy sources have posed significant challenges for improving the electric power transmission system. The point-to-point HVDC transmission links scattered around the world have been able to address some of the transmission challenges. In particular, from technical and economical points of view, point-to-point HVDC systems are considered attractive for integration of large-scale offshore wind farms and for reinforcement of interconnected regional power grids over AC transmission solutions. However, HVDC links have the limitation of exchanging power between only two terminals/points of connection to the AC grid. It is envisaged that multi-terminal DC (MTDC) grids with more than two terminals/converter stations can improve functionality, stability, and reliability of the power grid while decreasing the conversion losses and investment cost [22]. The strategic importance of MTDC grids is evidenced by the number of worldwide projects currently in their advanced planning stage, e.g., European " Supergrids " and the Baltic Sea project along with a few projects in China [22–24].

Amid the optimism surrounding the benefits of MTDC grids, their protection against DC-side faults remains one of their major technical challenges [24]. Proper protection of the MTDC grids necessitates the DC circuit breakers (CBs) to selectively and quickly isolate any faulty line without interrupting the entire system. Among the proposed DC CBs [26], the hybrid solid-state one is the most promising option as its breaking time is in the order of a few milliseconds while its conduction losses during normal operation are quite low [27].

Consisting of three paths, i.e., the nominal current path (NCP), the current commutation path (CCP), and the energy absorption path (EAP), a hybrid DC CB, as shown in Fig. 2.1, is designed to clear a fault through forcing the fault current from the NCP to the CCP and the EAP. During normal conditions, the current flows through the ultra-fast disconnector (UFD) and the load commutation switch (LCS) in the NCP. Subsequent to a fault, the fault current is routed to the CCP, which is comprised of a number of identical modules with parallel connected main breakers and arresters.

Once the CCP establishes a conducting path, the UFD opens. Conventionally, the opening of the UFD is followed by simultaneous tripping of all series-connected modules on the CCP and the EAP [26–29]. This tripping method results in a high voltage applied to the arresters, which are used to extinguish the fault current. However, this voltage introduces a high voltage stress across the UFD, which takes 2-3 ms to establish sufficient voltage withstand capability [29]. This delay ultimately limits the speed of the DC CB.

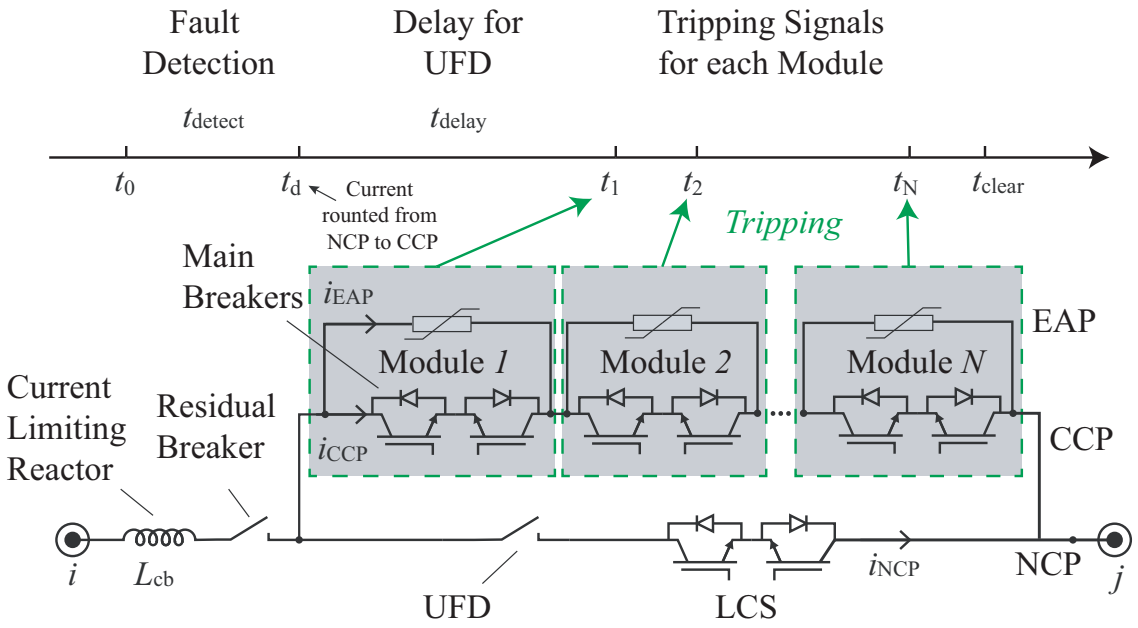

Figure 2.1: Circuit diagram of the hybrid DC circuit breaker [26].

To speed up the operation of hybrid DC CB and attenuate overcurrents and overvoltages, a sequential switching strategy is proposed in this report. This switching strategy enables a step-by-step tripping of breaker modules even before the UFD is fully opened. Based on the proposed approach, the fault is interrupted in an early stage by applying the voltage of the arrester banks within each breaker module in a progressive manner. This earlier interruption of fault reduces the rate of rise of fault current and, consequently, contributes to the attenuation of the overcurrent and overvoltage stresses as well as shorter fault clearance time. Nevertheless, the introduction of sequential tripping breaks the balance of energy distribution among the breaker modules. To relieve the energy stress applied on these modules, the tripping sequence is rescheduled. The ratings and tripping instants of breaker modules are then determined through an optimization method. An optimal design process is provided for recommending the best practice. To verify the benefits of the proposed sequential switching strategy, performance metrics indicating the current and voltage stresses are quantified through a time-domain analytical modeling approach considering travelling waves on DC transmission lines. The transient performance of the sequential tripping mechanism is confirmed based on both simulation studies in the PSCAD/EMTDC software environment and quantitative analysis.

2.2 The Proposed Sequential Switching

The hybrid DC CB, shown in Fig. 2.1, comprises the parallel connection of the NCP, which is formed by the LCS in series with the UFD, the CCP known as the main breaker, which consists of several modules, consisting of a number of series-connected semiconductor devices, and the energy absorption path (EAP), on which the arrester banks are deployed on the modules of the CCP to limit the voltage and absorb the residual energy when the main breaker is switched off. A series current limiting reactor L_{cb} is also connected in the CB to limit the rate of rise of the fault current.

To demonstrate the fault response subsequent to a DC side fault, a timeline is presented in Fig. 2.1. The fault current reaches the DC CB at the terminals of the faulty line at t_0. Upon detection of the DC-side fault at t_d and considering a detection delay of t_detect, the DC CB starts to isolate the faulty line. The LCS in the NCP is switched off subsequently to the closing of switches in the CCP to force the current to the CCP. Conventionally, a time delay is inserted to ensure successful opening of the UFD. The IGBTs within all N modules are then tripped simultaneously. The opening of these modules introduces a fast increased voltage across the breaker due to the release of energy stored in the circuit inductance [22]. This transient voltage exceeds the threshold voltage of the arresters until it is clamped by their highly nonlinear V-I characteristics. To ensure a successful operation of the NCP under high voltage stress, a certain delay t_delay has to be inserted before a sufficient voltage withstand capability is fully built up across the UFD [29–33]. This delay ultimately limits the speed of hybrid DC CB.

To expedite the operation of hybrid DC CB, a sequential switching strategy is proposed, in which the switches of the N modules in the main breaker are switched off sequentially. The opening of the breaker is divided into N stages. Consisting of semiconductor switches and their paralleled arresters, each module is treated as an individual breaker. These modules do not necessarily need to be tripped at the same time. Instead, the trip signals for them are generated sequentially at t_1, t_2 ... t_N. The arresters within these modules are rated at lower voltages, enabling them to introduce a lower voltage stress when inserted into the circuit individually. By tripping these modules sequentially, the voltage across the UFD is built up step by step. Since the voltage withstand capability of the UFD is established incrementally [29–33], the breaker modules can be tripped earlier, even before it is fully opened. For example, the switches of Module 1 are commanded to open at t_1, which is earlier than the original tripping instant in the conventional method. The fault current tends to increase slowly with the arresters in Module 1 been inserted. Sequentially, Module 2 is tripped at t_2, thereby the rate of rise of fault current is further limited. This process is repeated until all of the N modules are switched off, which allows the voltage across the hybrid CB to increase incrementally. Consequently, the fault clearance time can be reduced, and the overvoltage and the overcurrent stresses on the system are relieved as well.

The currents and voltages of the hybrid CB tested with simultaneous conventional and a four-stage sequential tripping strategies are shown in Fig. 2.2. A fault occurs at $t = 0\,\mathrm{ms}$ and reaches the CB at $t = 1.1\,\mathrm{ms}$. Upon fault detection at $t = 1.7\,\mathrm{ms}$, the current is routed from the NCP to the CCP. After 1.1 ms delay for the opening of UFD connectors, in sequential tripping case, the switches of Module 1 open 0.9 ms earlier than the simultaneous case. The voltage across the hybrid CB increases step by step with the sequential tripping of the modules. Compared to the abrupt voltage increase in simultaneous switching, the reduced voltage stress on the UFD allows the breaker to be opened earlier. Meanwhile, the fault current can be reduced since the voltage is applied earlier.

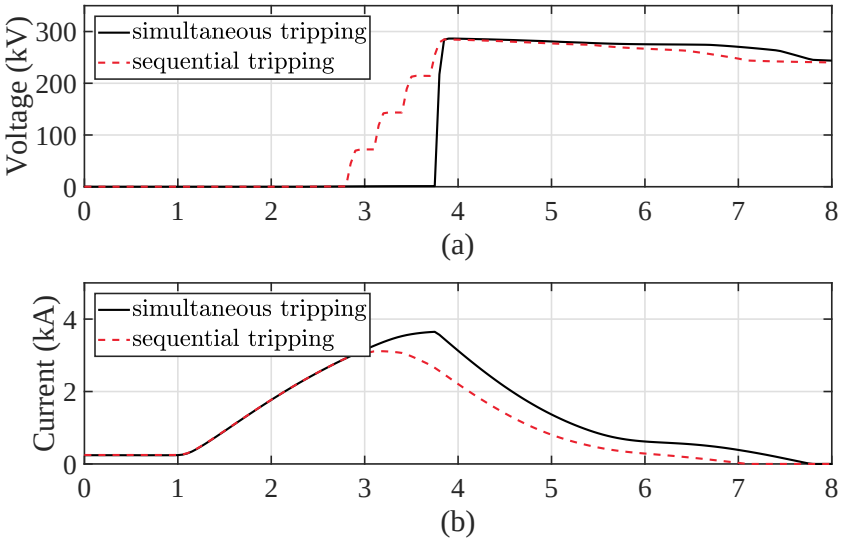

Figure 2.2: Simulated results in simultaneous and sequential tripping cases: a) voltage of the hybrid CB; and b) fault current.

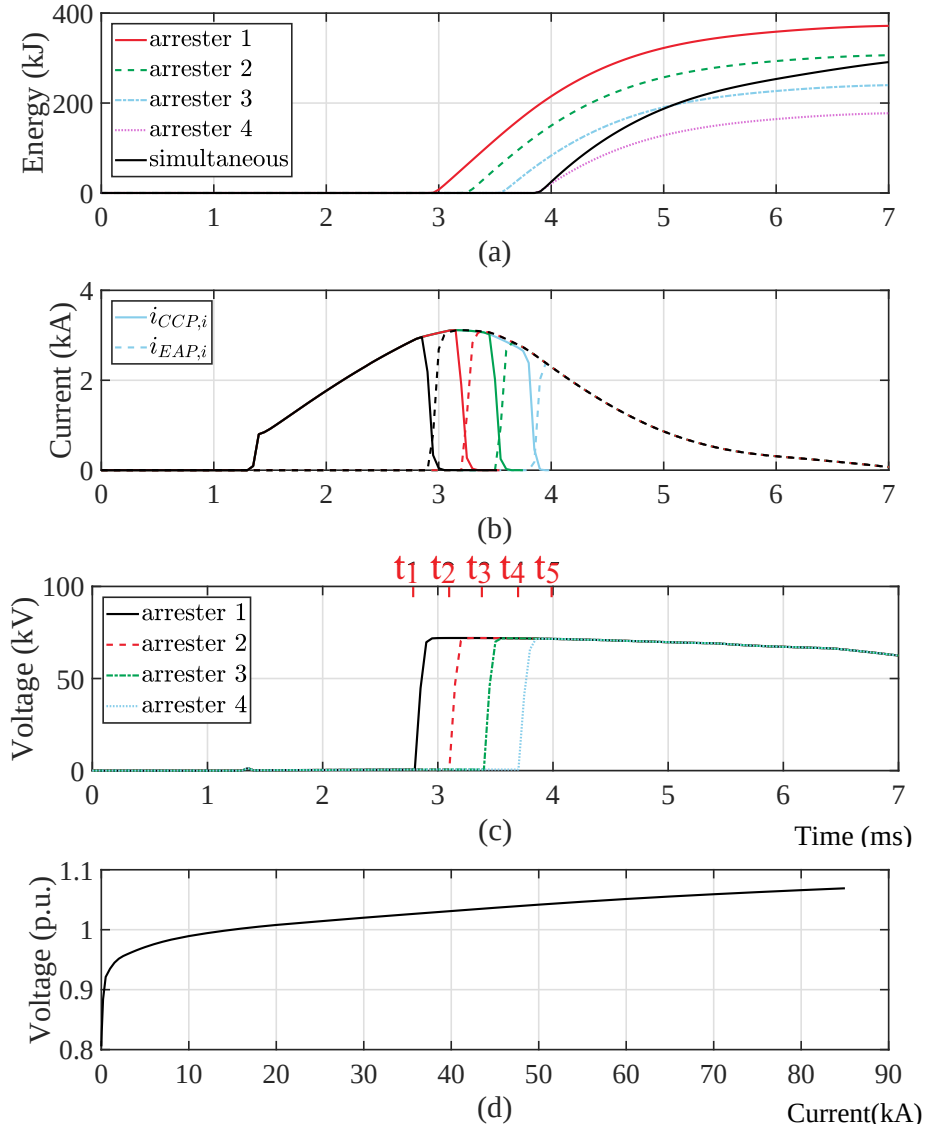

Figure 2.3: Simulated results of each module: a) currents of each module; b) voltage of various module arresters; c) absorbed energy by arresters and d) V-I characteristic of the arrester.

2.3 Energy distribution among arresters

Apart from the advantages offered by the sequential tripping, the energy absorbed by each module tends to be distributed unevenly, as shown in Fig. 2.3(a). Those modules that are tripped earlier tend to dissipate more energy, making them vulnerable to thermal overloading. Assuming that the clamped voltage of an arrester inside Module i is $v_{\mathrm{EAP},i}$ and the corresponding current is $i_{\mathrm{EAP},i}$, the energy absorption of the arrester i can be expressed by

$$W_{\mathrm{EAP},i} = \int_{t_i}^{t_{\mathrm{clear}}} v_{\mathrm{EAP},i} i_{\mathrm{EAP},i} dt, \tag{2.1}$$

where $W_{\mathrm{EAP},i}$ is the absorbed energy, and t_1 and t_2 are the starting and ending time instants of insertion of the arrester in Module i, respectively.

The current and voltage profiles of breaker modules tripped by the proposed strategy are provided in Figs. 2.3(b) and (c). Starting from the tripping of Module 1, the current does not substantially change till the opening process of all modules is completed. The voltage is also clamped at the same value by the non-linear V-I characteristic of the arrester, as shown in Figs. 2.3(d). Therefore, the absorbed energy of each arrester is largely proportional to the duration in which each of them is inserted into the circuit. The arrester within the earlier switched module absorbs more energy, as shown in Fig. 2.3(a). The energy difference is enlarged when a higher delay is applied between each module.

To address this issue, a modified sequential strategy is proposed to equally distribute the energy among all arresters, which adjust the sequence of the tripping to achieve equal inserting duration for each arrester [34]. t_i, $i \in [1,4]$, represent the time instants when the arresters 1 to 4 are tripped with the normal sequential tripping, as annotated in Fig. 2.3(c). Time t_5 is the instant when all four arresters are completely inserted. The periods t_1 to t_5 are evenly divided into 10 subintervals. The circle indicates the insertion of the corresponding arrester during the specific subinterval indicated on the left most column. In normal sequential tripping method, arrester 1 is inserted within all ten subintervals while arrester 4 is just inserted within two subintervals.

The modified strategy, which is provided in Table 2.1, controls the number of circles in each row such that the inserted voltage increases incrementally to clear the fault current. Meanwhile, the tripping sequence is redistributed in such a way that every arrester is inserted for the same duration of time (the summation of each column is the same) before t_5, from when all four arresters are inserted at the same time. Taking arresters 1 and 2 as an example, the absorbed energy of the original and modified sequential tripping strategies can be calculated by (2) and (3), respectively, as

$$\begin{aligned} W_{\mathrm{EAP},1} &= \int_{t_1}^{t_5} v_{\mathrm{EAP},1} i_{dc} dt, \\ W_{\mathrm{EAP},2} &= \int_{t_2}^{t_5} v_{\mathrm{EAP},2} i_{dc} dt. \end{aligned} \tag{2.2}$$

Table 2.1: Demonstration of the modified sequential tripping strategy [34].

	Original Sequential					Modified Sequential			
subinterval	1	2	3	4		1	2	3	4
$t_1 \sim {}^{(t_2-t_1)}/_2$	◯					◯			
${}^{(t_2-t_1)}/_2 \sim t_2$	◯					◯			
$t_2 \sim {}^{(t_3-t_2)}/_2$	◯	◯				◯	◯		
${}^{(t_3-t_2)}/_2 \sim t_3$	◯	◯			⇒			◯	◯
$t_3 \sim {}^{(t_4-t_3)}/_2$	◯	◯	◯				◯	◯	◯
${}^{(t_4-t_3)}/_2 \sim t_3$	◯	◯	◯				◯	◯	◯
$t_4 \sim {}^{(t_5-t_4)}/_2$	◯	◯	◯	◯		◯	◯	◯	◯
${}^{(t_5-t_4)}/_2 \sim t_5$	◯	◯	◯	◯		◯	◯	◯	◯

$$
\begin{aligned}
W_{\mathrm{EAP},1} &= \int_{t_1}^{(t_3-t/2)/2} v_{\mathrm{EAP},1} i_{\mathrm{dc}} dt + \int_{t_4}^{t_5} v_{\mathrm{EAP},1} i_{\mathrm{dc}} dt, \\
W_{\mathrm{EAP},2} &= \int_{t_2}^{(t_3-t/2)/2} v_{\mathrm{EAP},2} i_{\mathrm{dc}} dt + \int_{t_3}^{t_5} v_{\mathrm{EAP},2} i_{\mathrm{dc}} dt.
\end{aligned} \tag{2.3}
$$

Since the eight subintervals are equally divided, the energy absorbed by Module 1 and Module 2 are close, as indicated by $W_{\mathrm{EAP},1}$ and $W_{\mathrm{EAP},2}$ in (2.3). In this way, the energy distribution is significantly improved.

2.4 Tripping signal optimization

Based on the aforementioned modified strategy, the energy of the arresters can be theoretically distributed evenly to avoid any thermal overload. However, the fault current does not strictly remain the same during the opening of the modules as assumed. The energy difference among modules still exists, demanding further improvement of this tripping strategy. Moreover, the rated voltage of arresters and the tripping intervals between each module do not necessarily need to be the same. These parameters are to be determined in such a way that the voltage withstand capability established by the UFD can be optimally utilized at every instant. While ensuring successful opening of each module, this optimization makes a further improvement on transient performance.

The voltage withstand capability of the UFD is a function of time largely determined by its contact travel curve and insulation medium [29–33]. This capability is built up with the increment of distance between the contacts [33, 35]. The opening speed of the contacts varies for different UFDs. The detailed discussion on this topic will be presented in a future work. In this report, a non-decreasing characteristic of the UFD is generally assumed and depicted in Fig. 2.4. At the time Module i opens, the inserted voltage established by the arresters is applied to the UFD. At this moment, the corresponding voltage withstand capability of the UFD should be higher than this voltage. As shown in Fig. 2.4, the tripping schedule is determined by both the rated voltages u_{r} and tripping stages N. These two parameters will ultimately influence the system performance

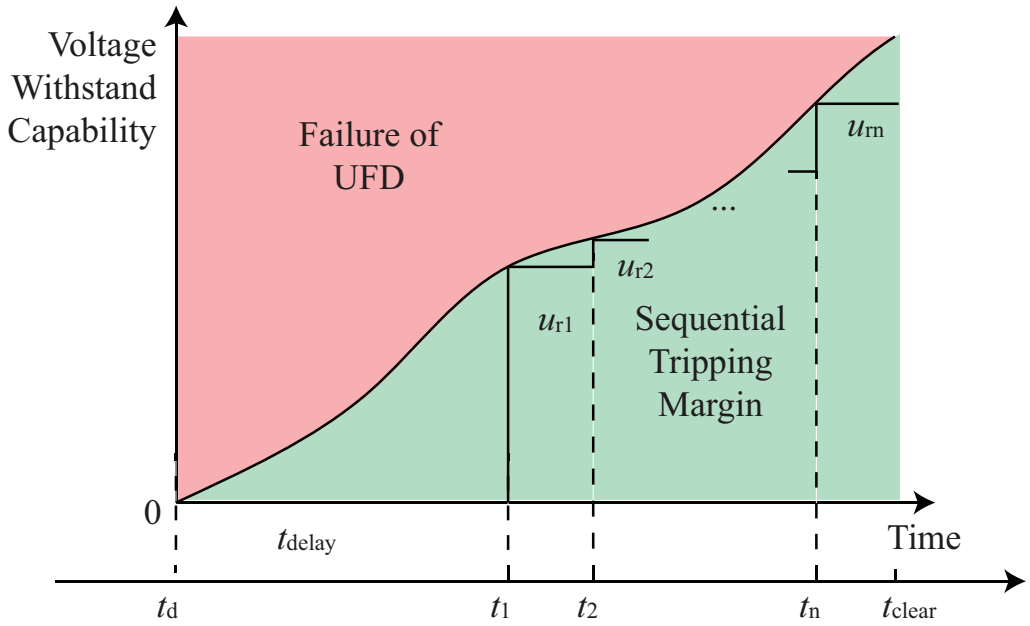

Figure 2.4: Generic voltage withstand capability versus opening time of the UFD.

metrics, i.e., fault clearance time, overcurrent, overvoltage, and energy absorption.

Typically, a module with a smaller u_r can be tripped earlier provided that a smaller additional withstand capability is required. However, this will result in an increment of the tripping stages. A large number of stages will add to the complexity of the controller and will potentially lead to a higher overvoltage. Additionally, the clearance time cannot be further improved with too many stages involved. To this end, the parameters of the sequential tripping should be selected wisely considering the trade-offs between different system metrics. An optimization should be performed to achieve such a balance. In a real application, it is likely that the arresters within the breaker modules are rated at the same level, for the sake of the simplicity of manufacturing maintenance. On the other hand, these arresters could be rated at different levels from an economical perspective. In this report, two optimization approaches are provided with respect to these considerations.

2.4.1 Approach 1

In the first approach, the rated voltage of the arresters of all modules are set to be same. The task is then to minimize the system performance metrics with respect to this rated voltage u_r and the number of tripping stages N.

In case u_r and N are selected, the earliest tripping instants of each module, t_i can be determined from the characteristic of the UFD. To prevent the UFD from failure, Module i should not be opened until the UFD is able to withstand the voltage inserted by the arresters. As shown in Fig. 2.4, at each instant t_i, an additional voltage u_{ri} is added on top of the previously accumulated voltage through the insertion of Module i. Intuitively, the earliest trip instant of Module i is the

moment when this accumulated voltage curve intersects with the UFD characteristic curve. With this approach, t_i can be written as

$$t_i = f_1(u_\mathrm{r}, N). \tag{2.4}$$

The expressions of the current flowing through DC CB, i_dc and the voltage across DC CB, v_dc are given as

$$i_\mathrm{dc} = f_2(u_\mathrm{r}, N) \tag{2.5a}$$
$$v_\mathrm{dc} = f_3(u_\mathrm{r}, N), \tag{2.5b}$$

where these transient functions can be obtained through the time-domain calculation method proposed in this report, as described in detail in Section V. In this way, the system metrics, i.e., peak overcurrent i_max, peak overvoltage v_max, fault clearance time t_clear, and energy absorption W_sum, are given as functions of u_r and N as

$$i_\mathrm{max} = g_1(u_\mathrm{r}, N), \tag{2.6a}$$
$$v_\mathrm{max} = g_2(u_\mathrm{r}, N), \tag{2.6b}$$
$$t_\mathrm{clear} = g_3(u_\mathrm{r}, N), \tag{2.6c}$$
$$W_\mathrm{sum} = \sum_{k=1}^{N} W_{\mathrm{EAP},i} = g_4(u_\mathrm{r}, N). \tag{2.6d}$$

Each of the four metrics can be used as the objective function for the optimization problem formulated in (2.7).

$$\underset{u_\mathrm{r}, N}{\text{minimize}} \quad g(u_\mathrm{r}, N) \tag{2.7a}$$
$$\text{subject to} \quad N_\mathrm{min} \leq N \leq N_\mathrm{max}, \tag{2.7b}$$
$$u_\mathrm{r,min} \leq u_\mathrm{r} \leq u_\mathrm{r,max}, \tag{2.7c}$$
$$u_\mathrm{r} \cdot N \leq u_\mathrm{r,sys}, \tag{2.7d}$$

where $g(u_\mathrm{r}, N)$ represents one of the system metrics in equation (2.6). Inequalities (2.7b) and (2.7c) ensure N and u_r stay within their reasonable limits. The total rated voltage of the DC CB is limited by the insulation capability of the system, $u_\mathrm{r,sys}$. This constraint is given by (2.7d).

A set of u_r and N is obtained by solving the optimization problem (2.7). However, the energy among N modules are not strictly balanced using the modified sequential tripping strategy. Considering that the tripping intervals are not necessary to be same, the $N-1$ tripping instants t_2, t_3, ..., t_N are open to be manipulated around the previous values to balance the energy. Given u_r and N, each $W_{\mathrm{EAP},i}$ can be written as a function of t_2, t_3, ..., t_N. Solving a set of $N-1$ energy balancing equations $W_{\mathrm{EAP},i} = W_{\mathrm{EAP},i+1}, i \in \{1, ..., N-1\}$ with respect to the $N-1$ tripping instants, the energy of each module is kept equal.

2.4.2 Approach 2

In some cases, the arrester within each module can be sized in such a way that the cost is minimized. The ratings of these arresters can thus be determined individually as $u_{\mathrm{r},1}$, $u_{\mathrm{r},2}$, ..., $u_{\mathrm{r},N}$. It is assumed that the summation of all rated voltages is $u_{\mathrm{r,sys}}$ and the number of tripping stage N is fixed.

Based on the time-domain calculation method provided in Section V, the four system metrics can be written as functions of the rated voltage of each arrester. The optimization problem is formulated as

$$\underset{u_{\mathrm{r},1},\ldots,u_{\mathrm{r},N}}{\text{minimize}} \quad h(u_{\mathrm{r},1},\ldots,u_{\mathrm{r},N}) \tag{2.8a}$$

$$\text{subject to} \quad \sum_{k=1}^{N} u_{\mathrm{r},k} = u_{\mathrm{r,sys}}, \tag{2.8b}$$

$$u_{\mathrm{r,min}} \leq u_{\mathrm{r},k} \leq u_{\mathrm{r,max}}, k \in \{1,\ldots,N\}, \tag{2.8c}$$

where $h(u_{\mathrm{r},1},\ldots,u_{\mathrm{r},N})$ represents one of the system metrics with respect to $u_{\mathrm{r},i}$.

2.5 Time-domain Transient Calculation

To optimally size the parameters of the proposed sequential tripping method, the functions g and h appeared in the optimization problems in (2.7) and (2.8) are derived by a time-domain calculation method in this report. This method, based on the concept of traveling waves, can be used to analyze the transient performance of the sequential switching hybrid DC CB in an MTDC system. In this report, pole-to-pole faults are assumed, which are more severe among DC-side faults.

When a pole-to-pole fault occurs on the line connected to one bus of the MTDC grid, the fault current is contributed by all adjacent branches, including adjacent lines and the converter connected to the same bus with the faulty line. Based on the concept of traveling waves, the equivalent circuit at the terminal of the faulty line is shown in Fig. 2.5. The line is represented by its characteristic impedance Z_0 with the limiting reactor L_{cb} in series with the DC CB.
The equivalent model of the converter is based on its blocking stage. Prior to its blocking, the converter is equivalent to an R-L-C circuit, of which the discharging of the capacitor contributes to the increase of the fault current. Once the IGBTs of the converter are blocked, the flowing path of the arm current determines the output voltage of the converter.
According to the conducting of the arm currents at each stages of the blocking converter [36], the converter becomes equivalent to

$$U_{\mathrm{CON}} = \begin{cases} 0, & t \in [t_{\mathrm{b1}}, t_{\mathrm{b2}}] \\ 3/2U_{\mathrm{pnu}}, & t \in [t_{\mathrm{b2}}, t_{\mathrm{b3}}] \end{cases}, \tag{2.9}$$

where t_{b1} and t_{b2} are the beginning of each stage of blocking converter, U_{pnu} is the peak value of phase-to-neutral voltage of AC voltage. The DC breaker can open at any stage of converter blocking according to the delay time t_{delay} of the UFD, so the transients can be calculated based on the corresponding model of the converter.

The equivalent model of the sequentially switched hybrid CB with N modules is included in the circuit, which represents the moment when Module i opens, where i dynamically increases from 1 to N as the modules in the breaker are switched. When each module of the CCP is switched off, the current is forced from the breaker to the corresponding arrester and the voltage across the breaker rises very fast until it is clamped by the arrester. These tripped CCP switches along with their parallel-connected snubber circuits in each module are modelled as an equivalent capacitor and a reactor in parallel with the arrester. Once the current through the switches reaches zero, only the arrester remains in the circuit. The arrester is modelled by a nonlinear resistor, as provided in the PSCAD software by [37]:

$$i_{\mathrm{f,EAP}m} = f_{\mathrm{EAP}}(u_{\mathrm{EAP}m}), m = 1, 2, ..., i, \tag{2.10}$$

where the function f_{EAP} represents a piece-wise linear relationship between the current $i_{\mathrm{f,EAP}m}$ and voltage $u_{\mathrm{EAP}m}$ of arrester. The sequential switching of the CB continuously adds a new equivalent model of modules in the circuit until all the modules are turned off. The equations governing the breaker transient behavior when Module i is switched off are

$$i_{\mathrm{f,1}} = i_{\mathrm{f,CCP}i} + i_{\mathrm{f,EAP}i}, \tag{2.11a}$$

$$i_{\mathrm{f,CCP}i} = C_{\mathrm{CCP}i}\frac{\mathrm{d}u_{C_{\mathrm{CCP}i}}}{\mathrm{d}t}, \tag{2.11b}$$

$$u_{\mathrm{EAP}i} = L_{\mathrm{CCP}i}\frac{\mathrm{d}i_{\mathrm{f,CCP}i}}{\mathrm{d}t} + u_{C_{\mathrm{CCP}i}}, \tag{2.11c}$$

$$u_{\mathrm{EAP}} = \sum_{m=1}^{i} u_{\mathrm{EAP}m}. \tag{2.11d}$$

The transient behavior of the system can be expressed as

$$2u_{\mathrm{q}} = u_{\mathrm{EAP}} + Z_0 i_{\mathrm{f,1}} + L_{\mathrm{cb}}\frac{\mathrm{d}i_{\mathrm{f,1}}}{\mathrm{d}t} + u_{\mathrm{bus}}, \tag{2.12a}$$

$$u_{\mathrm{bus}} = Z_{\mathrm{aj}}\sum i_{\mathrm{f},j} + L_{\mathrm{aj}}\frac{\mathrm{d}\sum i\mathrm{f}, j}{\mathrm{d}t} = L_{\mathrm{CON}}\frac{\mathrm{d}i_{\mathrm{f,CON}}}{\mathrm{d}t} + R_{\mathrm{CON}}i_{\mathrm{f,CON}} + u_{\mathrm{CON}},$$

where u_{bus} represents the voltage at the busbar and u_{q} is the sum of all created incident traveling waves at the terminal of the faulty line. L_{aj} and Z_{aj} represent the equivalent inductance and

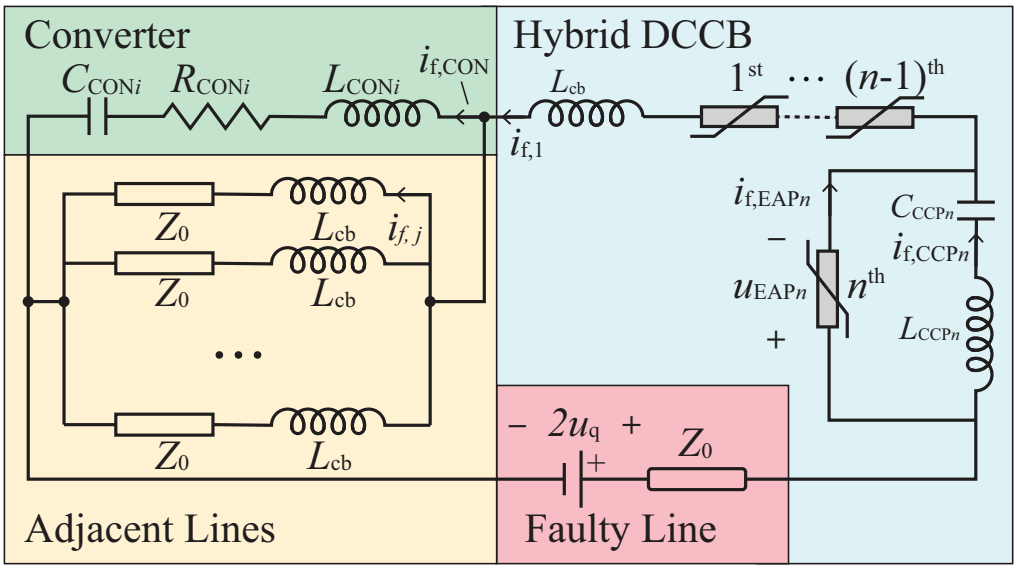

Figure 2.5: Equivalent circuit of the terminal of the faulty line.

impedance of the parallel adjacent lines.

The expression of the first surge voltage traveling on the faulty line can be solved from the telegrapher's equation of the traveling wave considering the skin effect at high frequencies [38]:

$$u_{q1}(z,t) = U_0 \cdot \mathrm{erfc}\left(\frac{k}{4L\sqrt{t - z/c}} \cdot \frac{z}{c}\right) \cdot u\left(t - \frac{z}{c}\right), \tag{2.13}$$

where $c = 1/\sqrt{LC}$ is the propagation speed of the line, $u(t)$ is a step function and $\mathrm{erfc}(t)$ is the complementary error function.

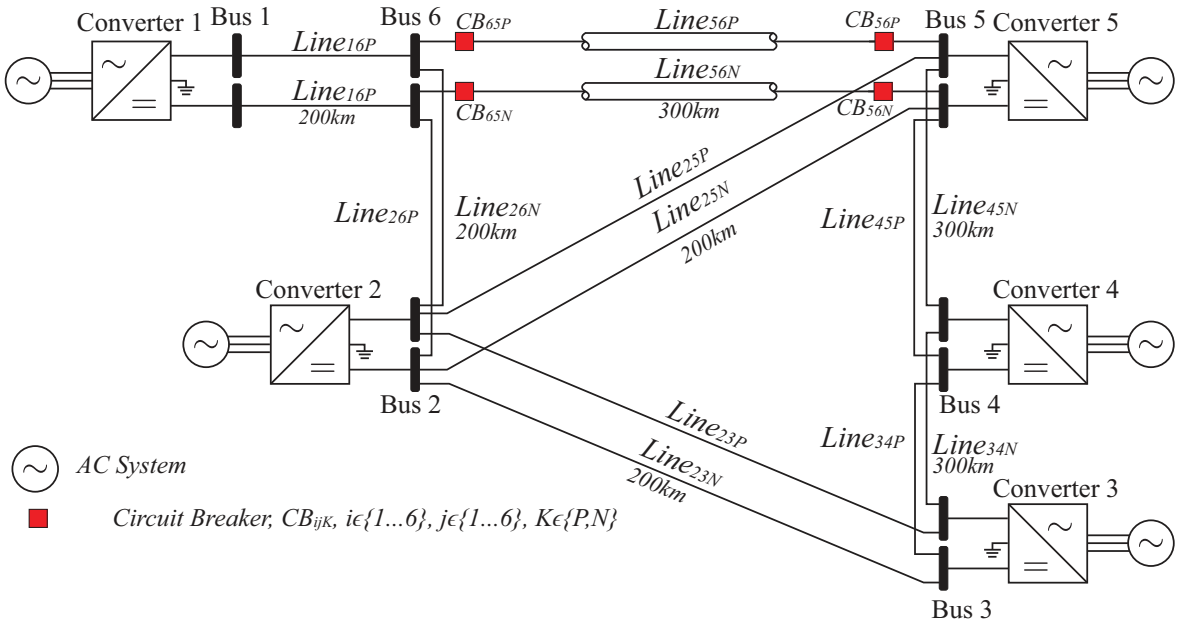

Figure 2.6: Layout of the five-terminal HVDC system [39, 40].

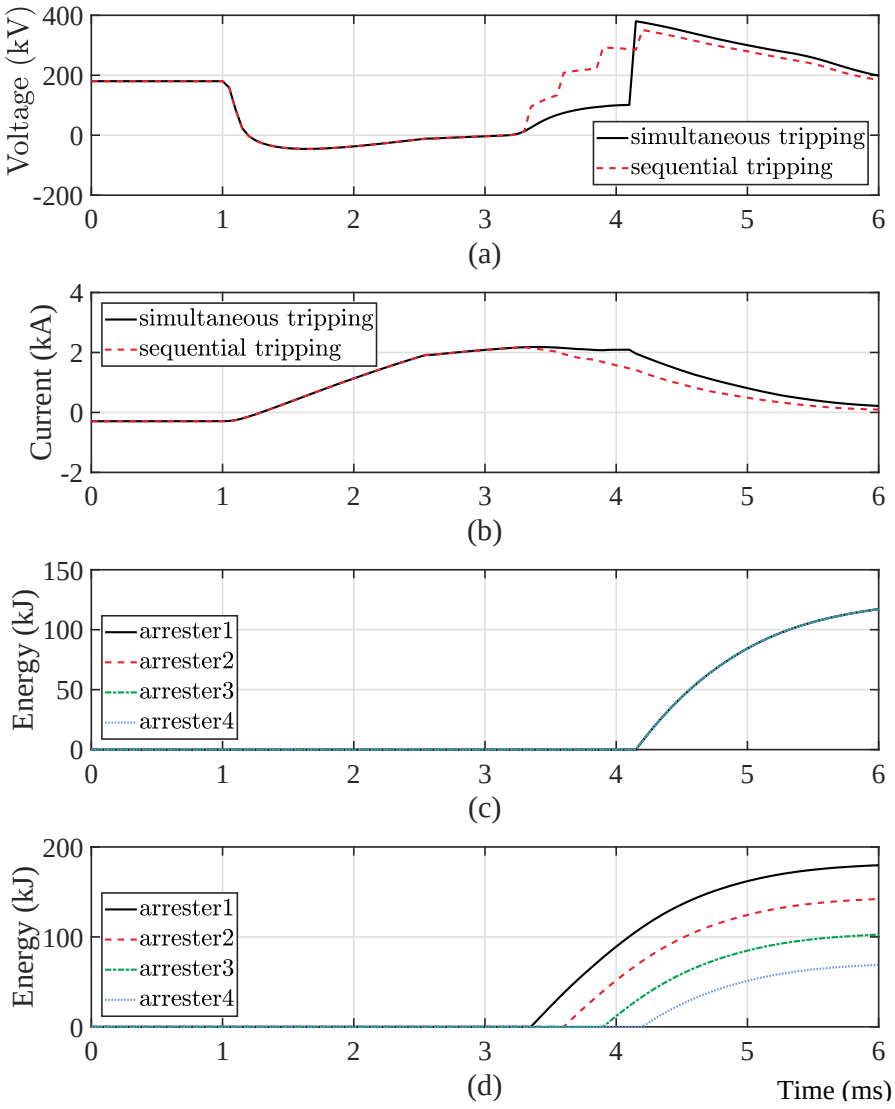

Figure 2.7: Transients of simultaneous and sequential tripped hybrid CBs: a) bus-side voltage of the breaker, b) fault current, c) absorbed energy of arresters for simultaneous case and d) absorbed energy of arresters of sequential case.

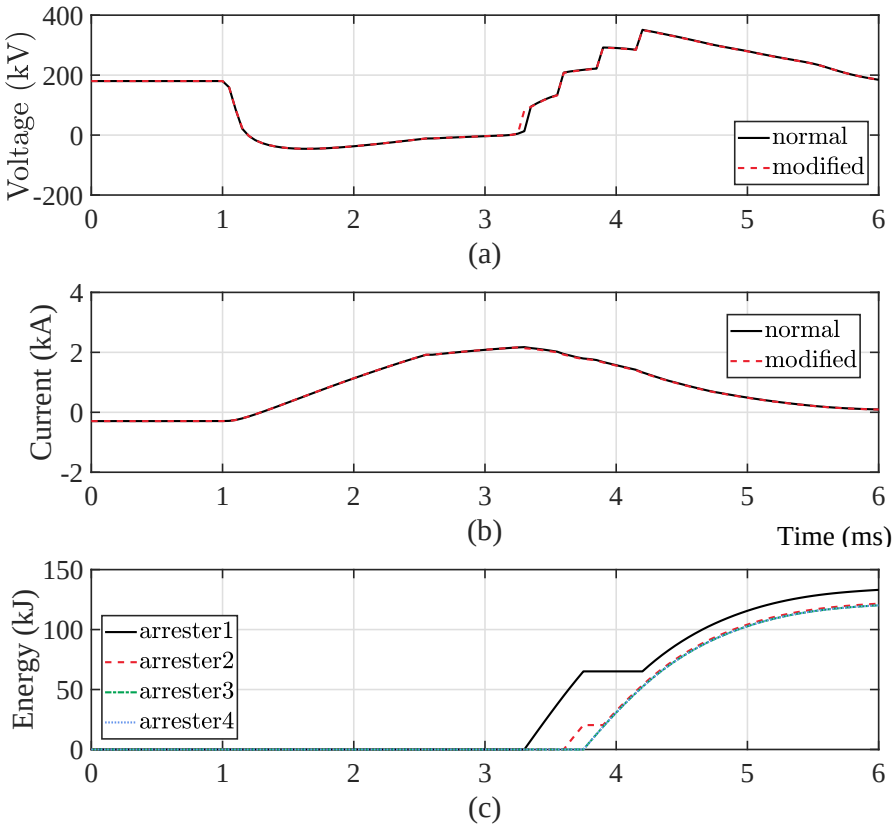

Figure 2.8: Transients of the modified sequentially tripped hybrid CB: a) bus-side voltage, b) fault current and c) absorbed energy.

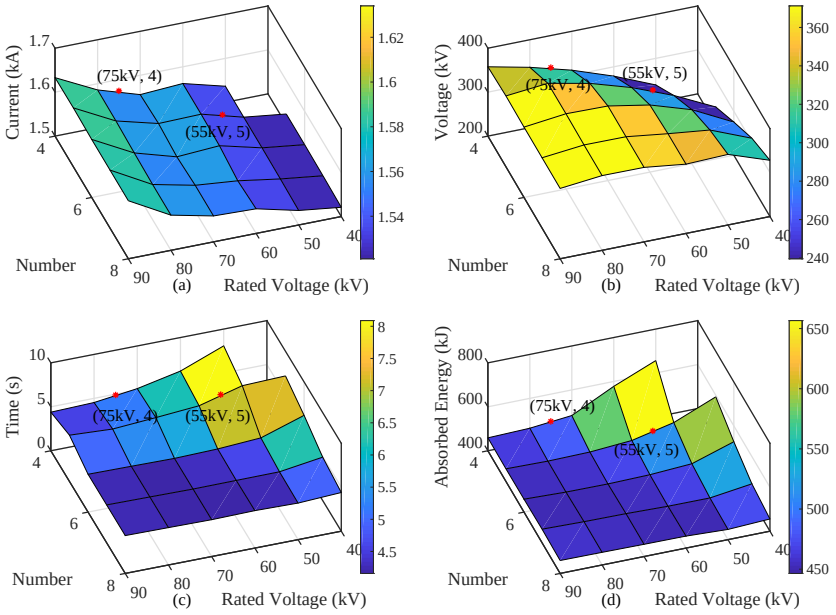

Figure 2.9: Fault transient performance variation versus u_r and N: a) maximum fault current, b) maximum overvoltage c) clearance time and d) absorbed energy.

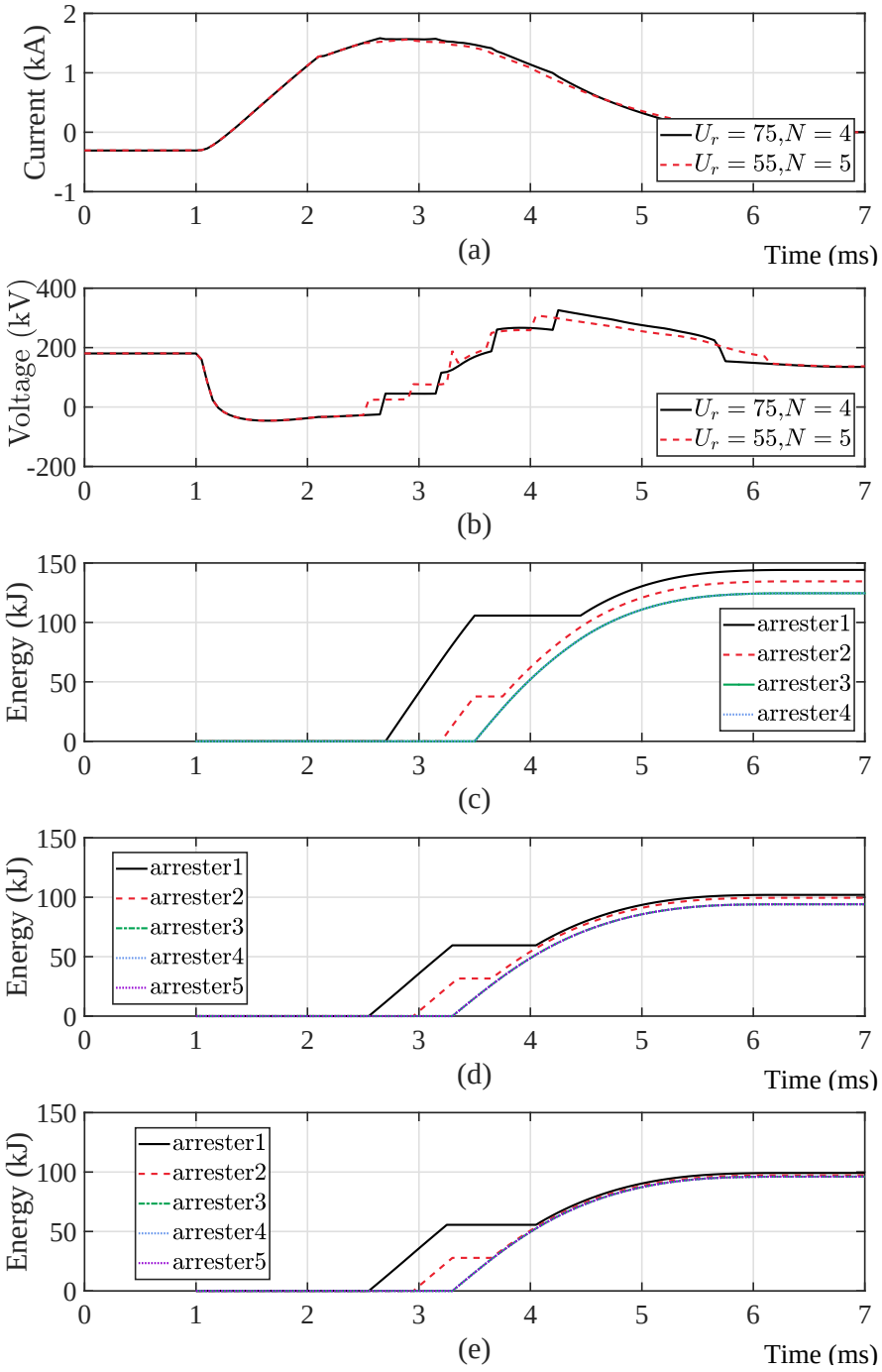

Figure 2.10: Simulation results of the selected scenarios: a) fault current, b) bus-side voltage, c) absorbed energy in scenario (i), d) absorbed energy in scenario (ii), and e) absorbed energy with updated time instants.

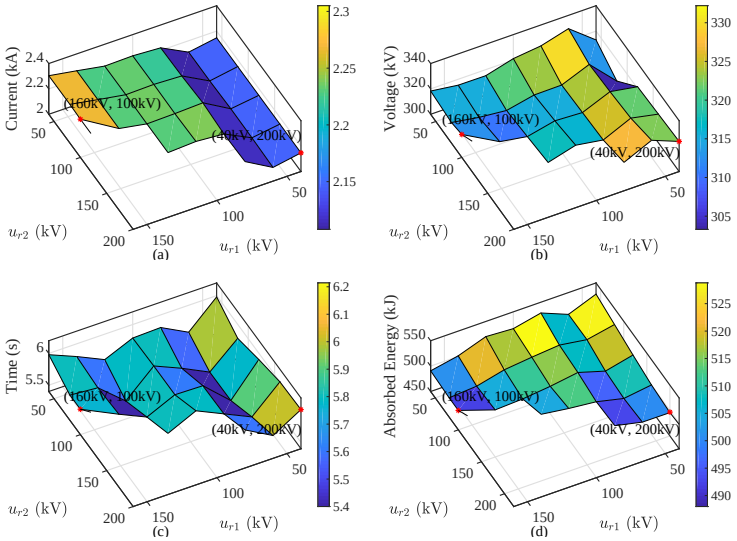

Figure 2.11: Fault transient performance variation versus u_{r1} and u_{r2}: a) maximum fault current, b) maximum overvoltage c) clearance time and d) absorbed energy.

Based on the first incident voltage, the reflection coefficient at the terminal of the faulty line Γ_1 is fitted by the reflected voltage solved from the equivalent circuit as shown in Fig. 2.5, where the module number i can be set as 0, corresponding to the time interval before the breaker starts to operate. Then, for a fault located at a distance l from the terminal of the faulty line, the superposition of subsequent traveling waves created by the multiple reflects, u_{q} can be estimated by

$$\Gamma_1 = \frac{u_{\mathrm{f1}}}{u_{\mathrm{q1}}} = \frac{u_{\mathrm{t1}}}{u_{\mathrm{q1}}} - 1, u_{\mathrm{t1}} = u_{\mathrm{q1}} - Z_0 \cdot i_{\mathrm{f},1}, \tag{2.14}$$

$$u_{\mathrm{q}} = \sum_{m=0}^{\infty} u_{\mathrm{q1}}(l + 2ml, t)(\Gamma_1 \Gamma_2)^m, \tag{2.15}$$

where u_{f1} is the reflected backward voltage and u_{t1} is the refracted voltage transmitted into the terminal. The voltages and currents of the system during sequential switching can be computed by solving (2.10) to (2.12) with the superposition of all the incident waves u_{q}. This analytical calculation can be used to represent the fault performance and compute the maximum current and voltage as well as the fault clearance time during a pole-to-pole fault.

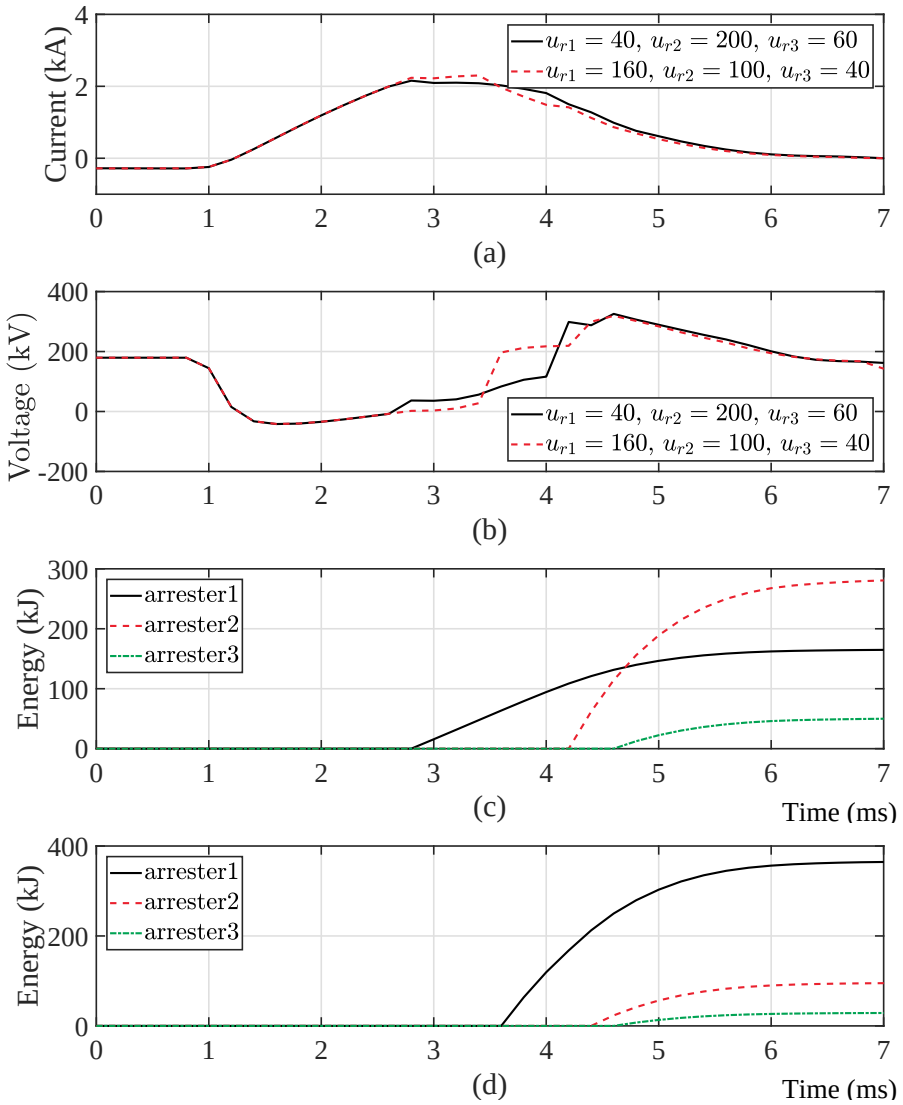

Figure 2.12: Simulation results of the selected scenarios: a) fault current, b) bus-side voltage c) absorbed energy in scenario (i), and d) absorbed energy in scenario (ii).

2.6 Results

Fig. 2.6 shows the layout of the test system adopted in this report. The test system, which represents a ± 200 kV five-terminal symmetric monopole meshed HVDC grid, is built with reference to CIGRE benchmark model [39]. The transmission lines include $Line_{34}$, $Line_{45}$, $Line_{56}$ with 300 km length, and the rest of the lines with 200 km length. DC CBs are located at both ends of each HVDC link. The detailed configuration of $Line_{56}$ is depicted in Fig. 2.6(a) while other lines use a simplified representation. The VSC stations are based on the well-known Modular Multilevel Converters (MMCs) [40]. Each station is grounded by a star point reactor on AC side to keep the DC voltage balance. The system parameters are provided in Table 2.2.

In this section, the proposed sequentially tripping strategy is verified in this test system in the

PSCAD/EMTDC software environment. The arrester is modeled using the V-I characteristic shown in Fig. 2.3(d). The transient performance of the proposed sequentially switched hybrid CB is compared with the conventional one. Based on the calculation results of the optimization problem, the parameters of the proposed tripping strategies are optimally sized through the two approaches described in Section 2.4. The results of optimization are also evaluated by simulations in this section.

2.6.1 Base Case

The base case is tested on $Line_{45N}$ where the positive and negative poles are shorted at 200 km away from Bus 4. The operation of hybrid DC CB are tested by both simultaneous and sequential tripping strategies. The waveforms of the currents and voltages, as well as the energy absorptions are compared in Figs. 2.7(a)-(d). This pole-to-pole fault occurs at $t = 0$ and reaches the terminal at $t = 1.1$ ms. When the fault is detected at $t = 2.2$ ms, the LCS opens to force the current to the CCP of the CB. In the simultaneous case, 2 ms is left for full opening of the UFD to withstand transient recovery voltage of 1.5 p.u. For the four-stage sequential tripping CB, the trip signal for the first stage is generated at $t = 3.3$ ms, i.e., 0.9 ms earlier than the simultaneous tripping CB, while the delay time for each stage is 0.3 ms.

Compared to the abrupt increase of voltage in the simultaneous tripping case, the bus-side voltage of four-stage CB increases incrementally and is clamped by the arrester at each stage, as shown in Fig. 2.7(a). The modules can be tripped earlier since the voltage across the UFD is applied step by step. This voltage helps reduce the voltage across the DC reactor and, consequently, reduce the rate of rise of fault current in the main circuit.

As shown in Fig. 2.7(b), the maximum current and the clearance time is reduced by sequentially switched hybrid CB as well. The maximum overvoltage of the system is also lower with the sequential tripped hybrid CB. However, compared to the balanced energy distribution of the arresters in simultaneous case in Fig. 2.7(c), the energy absorbed by the arresters in the sequential tripped modules is distributed unevenly. As shown in Fig. 2.7(d), the arresters within the earlier switched modules are inserted earlier in the circuit. These arresters tend to absorb more energy. Therefore, the proposed sequential tripping strategy should be updated to balance the energy distribution among modules.

Table 2.2: Converter and grid parameters,

	Conv. 1	Conv. 2-5
Rated capacity [MVA]	450	120
Rated DC Voltage [kV]	$\pm$200	$\pm$200
Rated AC voltage [kV]	220	220
Operation Mode Setpoints	$\pm$200 [kV]	$-$100 [MW]

2.6.2 Modified Sequential Case

To equally distribute the energy among the arresters in Fig. 2.7(d), the sequential tripping strategy is modified based on the proposed method in Section III. The tripping signals of the four-stage CB is rearranged as in Table 2.1, where the four arresters are inserted in the circuit for an equal duration.

The simulation results in the modified strategy are compared with the normal case in Fig. 2.8. The waveforms of currents and voltages in the modified case are close to the base case, which means that the modified sequential tripping reserves the benefits of the original strategy. The energy absorption in Fig. 2.8(c) shows that the modified strategy balances the energy distribution of the arresters within the sequentially tripped modules. This is further proved by the data in Table 2.3. However, since the fault current during each stage is not exactly the same, the first arrester absorbs more energy than the others.

Table 2.3: Absorbed energy by arresters

$W_{EAP,i}$ [kJ]	1	2	3	4
Normal strategy	117.7	88.9	60.6	36.7
Modified strategy	80.4	75.5	74.9	74.9

2.6.3 Optimized Sequential Strategy

Case 1: In the first optimization approach, the rated voltage, u_{r} of each module are set to be the same. It is assumed that the voltage withstand capability of the UFD is built up linearly to be 1.5 p.u. of the rated DC voltage at $t = 2\,\mathrm{ms}$. With the help of time-domain calculation, the four metrics of the fault performance, i.e, maximum overcurrent, maximum overvoltage, fault clearance time and absorbed energy with different combination of u_{r} and N are shown in Fig. 2.9.

With the increase of u_{r}, the minimum allowed time delay increases, resulting in higher maximum overcurrent, higher maximum overvoltage but shorter clearance time. With the same u_{r}, the fault current goes down to zero much faster and the maximum overvoltage becomes higher as N increases. However, the maximum overcurrent does not change much since the slope of fault current is changed in the same way. Similar to the trend of clearance time, the absorbed energy decreases while u_{r} and N increase. When N is too large, the fault is cleared before the last several modules are inserted. As a result, the absorbed energy remains unchanged when u_{r} and N are large enough.

The results in Fig. 2.9 can be used in the design process to determine the parameters to optimize any of the system metrics. u_{r} and N can be optimally selected based on the requirements of the system. Hereafter, two sets of parameters are selected to be compared by simulation studies: (i) $u_{\mathrm{r}} = 75\,\mathrm{kV}$, N= 4, and (ii) $u_{\mathrm{r}} = 55\,\mathrm{kV}$, N= 5. The transient performance of these two scenarios are compared in Fig. 2.10. The lower u_{r} in scenario (ii) allows the module to open earlier to limit

the fault current, resulting in a lower maximum overcurrent as shown in Fig. 2.10(a). The total inserted voltage and maximum voltage in scenario (i) are larger than scenario (ii) and, consequently, the clearance time is reduced. The total energy absorbed by the arresters in scenario (i) is 493 kJ, which is lower than 508 kJ of scenario (ii), as verified by Fig. 2.9(d).

As discussed in Section 2.4, the energy is not strictly balanced with the modified sequential tripping strategy. This can be observed from Fig. 2.9(d). Based on the values obtained from scenario (ii), the tripping instants are further improved to balance the energy. The updated energy distribution is plotted in Fig. 2.9(e).

Case 2: In the second optimization approach, a three-stage tripping strategy is applied while the total inserted voltage $u_{\mathrm{r,sys}}$ is set to be 300 kV. The transient performance of the system is calculated with different combinations of u_{r1}, u_{r2} and u_{r3}. The calculation results of the four metrics are plotted in Fig. 2.11. As shown in Fig. 2.11(a), the rated voltage of first arrester determines the maximum overcurrent during the operation of the DC CB. With lower u_{r1}, the Module 1 can be triggered earlier to limit the increase of the fault current and reduce the maximum overcurrent. The maximum voltage decreases as u_{r1} increases. When u_{r1} remains the same, the clearance time decreases and then increases while u_{r2} increases. The total energy absorbed by the arresters is also presented in Fig. 2.11(d), which tends to decrease with the increase of u_{r1} and u_{r2}.

This approach helps determine the parameters for those systems that are flexible in using different rated arresters. To demonstrate the design process, two scenarios are selected as following: (i) $u_{\mathrm{r1}} = 40\,\mathrm{kV}$, $u_{\mathrm{r2}} = 200\,\mathrm{kV}$, $u_{\mathrm{r3}} = 60\,\mathrm{kV}$; and (ii) $u_{\mathrm{r1}} = 160\,\mathrm{kV}$, $u_{\mathrm{r1}} = 100\,\mathrm{kV}$, $u_{\mathrm{r1}} = 40\,\mathrm{kV}$. The simulation results of the two scenarios are provided in Fig. 2.12. The system metrics are compared in these two scenarios. It is verified that the results presented in Fig. 2.11 provide a solid guidance for the design process.

In the second optimization approach, the ratings of the arrestors are considered to be non-identical. As a result, the voltages inserted into the circuit are not the same anymore. In this case, the energy distribution should no longer be balanced based on the same modified sequential strategy shown in Table 2.1. The arresters, which are rated at higher voltages and are tripped earlier, tend to absorb more energy as shown in Figs. 12(c) and (d).

2.7 Conclusion

In this report, a sequential tripping scheme for the hybrid CB is proposed to improve the DC fault transients in the MTDC grids. The proposed strategy sequentially trips the breaking modules within the CB to reduce the fault performance metrics including maximum fault current and fault clearance time compared to the conventionally tripped CBs. A modified sequential tripping strategy is then proposed to equally distribute the energy among the arresters. In addition, two approaches to optimally design the rating and determine the number of breaker modules are proposed to further improve the transient performance. Performance of the proposed sequential strategy is

verified by simulation studies conducted on an MTDC system based on the PSCAD/EMTDC software environment. Compared to the simultaneous tripping case, the sequential tripping strategy reduces the clearance time and relieves the overvoltage and the overcurrent stresses on the system. The energy distribution of the arresters among these modules is balanced by rescheduling the tripping sequence in the modified strategy. Finally, with the help of a time domain approach considering the traveling wave phenomenon, the rated voltage of the arresters and the number of the stages are optimally designed through two approaches and the selected scenarios are tested by simulations.

3. Optimum Selection of Circuit Breaker Parameters based on Analytical Calculation of Overcurrent and Overvoltage in Multi-terminal HVDC Grids

3.1 Introduction

The point-to-point High Voltage DC (HVDC) transmission is a mature technology with many installations around the world [41–43]. Over the past few years, the evolution of power electric converter technology has enabled the HVDC technology to further enhance reliability and functionality and reduce cost and power losses. Concomitantly, significant changes in generation, transmission, and loads such as integration and tapping renewable energy generation in remote areas, increasing transmission capacity, urbanization and the need to feed the large cities have emerged [42]. These new trends create the need for Multi-Terminal DC (MTDC) systems, which when embedded in the AC grid, can enhance stability, reliability, and efficiency of the present power grid [41].

Amid the optimism surrounding the benefits of MTDC grids, their protection against DC-side faults remains one of the major technical challenges. While the protection of two-terminal HVDC systems can be fulfilled by relying on converter controls and AC circuit breakers (CBs), proper protection of the MTDC grids necessitates the DC CBs to selectively isolate the faulty DC line/cable without interrupting the entire system. Among the proposed DC CBs [44], the hybrid solid-state CB [44, 45] is one of the most promising options as its current breaking time is in the order of a few milliseconds while its conduction losses during normal operation are low [44]. However, incorporating such DC CBs into the MTDC grid adds another level of complexity as the DC short circuit current increases with commensurate increase in transient overvoltage stress, current limiting reactor and energy absorption capability of arresters. To determine the fault clearing capability and performance of these DC breakers, there is a need for (i) an accurate method to estimate the maximum overcurrent, transient overvoltage stress and energy absorption, and (ii) an optimal parameter selection method to size the CB components to achieve satisfactory performance.

In calculating the fault response, several approaches have been proposed. A three-stage short-circuit current calculation method, using the lumped π-section cable model, is reported in [47,48]. Although the three-stage method is helpful to understand the behavior of the DC system after the fault, it is not sufficiently accurate within the first few milliseconds when the maximum fault current and over voltage occur. Considering the travelling wave phenomena, the authors in [49] derive the time-domain solutions of the fault current contributed by DC capacitors. Based on the response of frequency-domain models, fault behavior in multiple MTDC configurations have been studied in [50]. However, only the first travelling wave is taken into account in both [49] and [50]. Subsequent reflected and transmitted waves are important in estimating the maximum transient overvoltage. To this end, detailed and accurate calculation of subsequent traveling waves is necessary.

Once a quantitative estimation of maximum fault current, overvoltage, clearance time and energy absorption in arresters is obtained, optimum selection of the CB components can be attained. The authors in [51,52] investigate the operation of hybrid CBs and develop a parallel genetic algorithm in the MATLAB-EMTP environment to select breaker parameters. However, a large number of parallel processors are required to reduce the computation time even when dealing with simplified models of the point-to-point HVDC systems. This computation stress limits the applicability and expansion of the method to larger MTDC systems.

In this report, a time-domain approach is proposed to analytically calculate the transient response of the MTDC system during a DC fault by considering all the corresponding travelling waves. Based on the analysis, the fault behavior within the first few milliseconds is analytically modelled, and consequently, breaker parameters including operation delay, current limiting reactor and arrester can be optimally sized. In that regard, a multi-objective design optimization problem is formulated to explore the Pareto-optimal fronts of the transient response of the system versus the breaker parameters and to establish trade-offs among the breaker parameters and fault transient response. Finally, time-domain simulations in the PSCAD/EMTDC environment are performed to evaluate the accuracy and performance of the proposed method.

3.2 Test Multi-terminal HVDC System

Fig. 3.1(a) shows the layout of the test system adopted in this report. It represents a $\pm 200\,\text{kV}$ five-terminal symmetric monopole meshed HVDC grid, constructed from the CIGRE benchmark model [53]. The DC lines $Line_{34}$, $Line_{45}$, $Line_{56}$ are 300 km long while the rest are 200 km long. DC CBs are located at both ends of each HVDC link. In Fig. 3.1(a), for the sake of simplicity, the $Line_{56}$ is represented with its associated breakers at its two ends, while the other lines simply show the connections between the buses. The VSC stations use the well-known Modular Multilevel Converters (MMCs) [54].

The DC CBs, e.g., CB_{ijK}, used in the test system of Fig. 3.1(a) are based on the widely accepted hybrid solid-state CB [55] with a detailed model presented in Fig. 3.1(b). The breaker is mainly comprised of parallel connection of the nominal current path (NCP), which is formed by a load commutation switch (LCS) in series with an ultra-fast disconnector (UFD), the current commutation path (CCP), which consists of multiple semiconductor devices named the main breaker, and the energy absorption path (EAP), to limit the voltage and absorb the residual energy when the main breaker is switched off. A series-connected current limiting reactor L_{cb} is also included in the CB to limit the rate of rise of the fault current. The residual breaker is used to isolate the fault and to prevent the arrester banks from thermal overload.

Subsequent to a DC-side fault, upon detection of the fault, the breaker trip signal is generated. The LCS is blocked immediately and the current is forced to the main breaker. After a certain time delay for the UFD to establish voltage withstand capability, the main breaker is switched off and

the current is transferred to the EAP. Due to the energy stored in the circuit inductance, the voltage of main breaker increases very fast until it is clamped by the surge arrester. With the insertion of the arrester, the circuit impedance is increased and thereby the fault current is reduced.

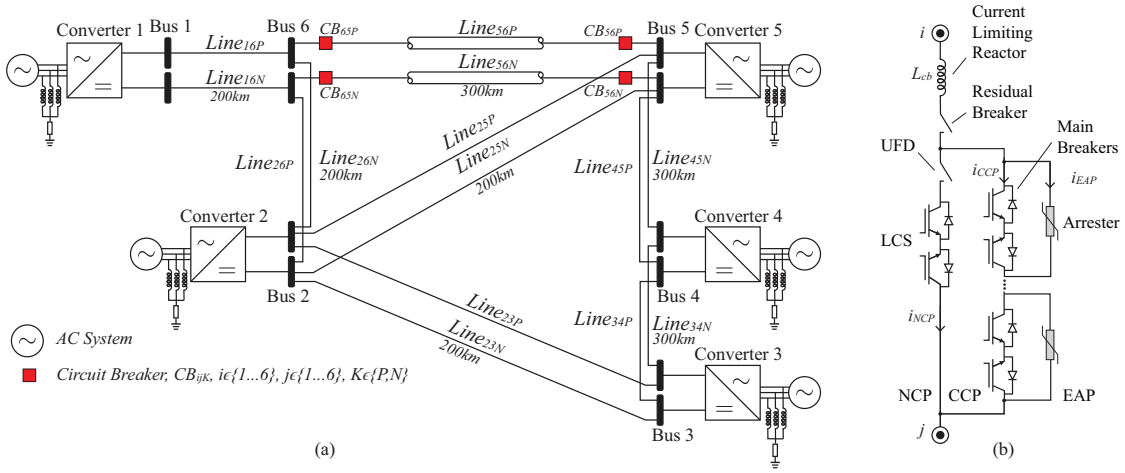

Figure 3.1: a) Layout of the MTDC grid test system and b) circuit diagram of the hybrid CB with its three paths.

3.3 Analytic Fault Transient Approximation

There are mainly two types of DC faults on the DC network, i.e., pole-to-ground and pole-to-pole faults. Compared to the former one, the latter is more severe because of its larger fault current [41, 50]. While the focus of this report is on a pole-to-pole fault, the analysis and developments are equally applicable to a pole-to-ground fault as well. Although the discharging circuit of a pole-to-ground fault is quite different, the principle and the method to build the equivalent circuit and the procedure to calculate fault transients for both cases are the same.

The layout of one terminal (Bus_i) of the MTDC grid is shown in Fig. 3.2. A pole-to-pole fault is assumed to be on cable $Line_{i1}$. The adjacent cables on Bus_i are denoted as $Line_{ij}, j \notin \{1,i\}$. The fault current, $i_{f,1}$ is broken down into two parts, i.e., $i_{f,CON}$ and $\sum_{j\notin\{1,i\}} i_{f,j}$, which are contributions from converter and adjacent cables, respectively. The incident surge e_i is transmitted to Bus_i and reflected as e_r, resulting in a fast voltage drop on the terminal. The detailed analysis of this traveling wave phenomenon, which has a significant impact on fault transients, is presented as follows.

3.3.1 Frequency-domain Expression of Traveling Waves

When the positive and negative poles are shorted at a certain distance from the terminal of the transmission line, the voltage surge generated at the fault location starts travelling to both ends of the faulty line. For a uniformly distributed lossy transmission line, the relationship of voltage $v(z,t)$ and current $i(z,t)$ at position z from the fault location is described by telegrapher's equations. In frequency domain, they yield the second-order differential equations expressed by:

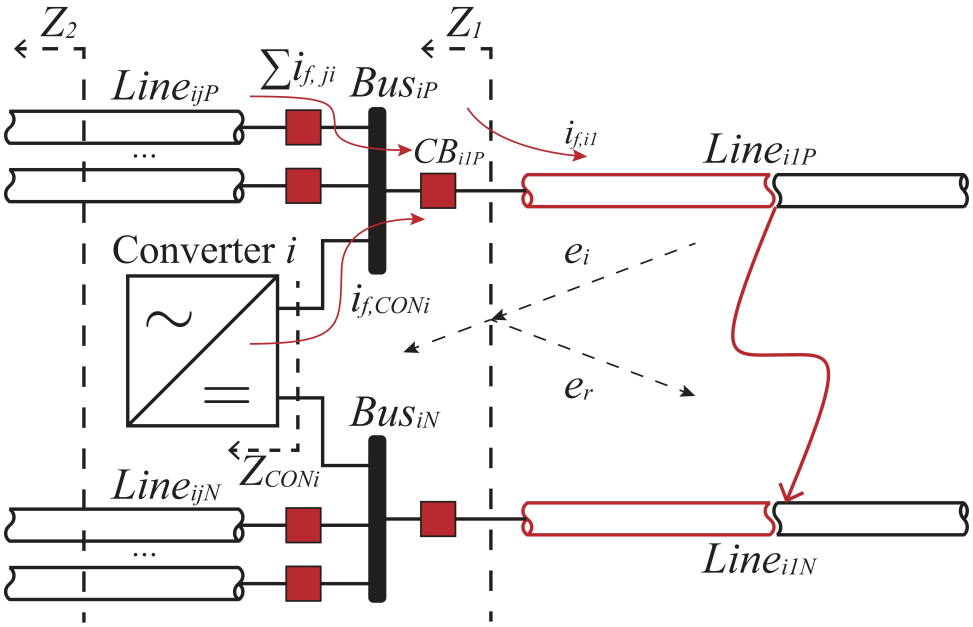

Figure 3.2: Fault current contributions during a pole-to-pole fault at Bus_i.

$$\frac{d^2V(z)}{dz^2} = \gamma^2(s)V(z), \tag{3.1}$$

$$\frac{d^2I(z)}{dz^2} = \gamma^2(s)I(z), \tag{3.2}$$

where $\gamma = \sqrt{Z(s)Y(s)}$ is the propagation constant of the transmission line. $Z(s)$ and $Y(s)$ are line series impedance and shunt admittance, respectively. The solution to (3.1) and (3.2) is

$$V(z) = V^+(z) + V^-(z) = V_0^+ e^{-\gamma z} + V_0^- e^{+\gamma z}, \tag{3.3}$$

$$I(z) = I^+(z) + I^-(z) = \frac{V_0^+}{Z_0} e^{-\gamma z} - \frac{V_0^-}{Z_0} e^{+\gamma z}, \tag{3.4}$$

where $Z_0(s) = \sqrt{Z(s)/Y(s)}$ is the characteristic impedance of the transmission line. Equations (3.3) and (3.4) are general expressions for traveling waves. $V^+(z)$ and $V^-(z)$ represent the forward and backward waves at point z, respectively.

The fault generated traveling waves include high-frequency components. A reasonable approximation of cable impedance is $Z(s) = L \cdot s + K\sqrt{s}$, where K is the skin effect factor [55]. The shunt capacitor C is constant and the inductance is assumed constant at high frequencies.

Assuming an initial voltage step V_0 at the fault location on an infinite-length cable, the backward wave V^- is zero while the incident wave can be expressed by [56]:

$$V_1^+(z) = \frac{V_0}{s} \exp\left(\frac{-z}{c}s - \frac{Kz}{2Lc}s^{1/2}\right), \tag{3.5}$$

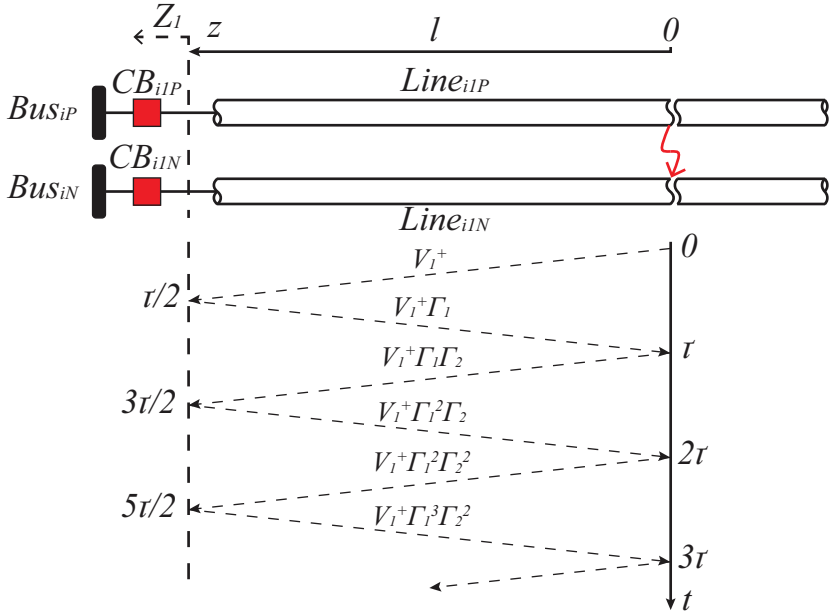

Figure 3.3: Lattice diagram for traveling waves of a faulty cable.

where $c = 1/\sqrt{LC}$ is the propagation speed of the cable [49].

With the first incident wave described by (3.5), the subsequent traveling waves on a finite-length cable can be also derived. The fault generated incident wave will be reflected at the terminal because the impedance changes to Z_1, including the series current limiting reactor L_{cb} in the DC CB and the equivalent impedance seen by the terminal. This reflected wave will be reflected again once it arrives at the fault location. These reflections are depicted in the lattice diagram in Fig. 3.3. Thus, within the first few milliseconds when the breaker has not opened yet, the voltage at the breaker, $V_{i1}(l)$, can be expressed as the superposition of several forward and backward traveling waves as

$$V_{i1}(l) = \sum_{m=0}^{\infty} V_1^+(l)(1+\Gamma_1)(\Gamma_1\Gamma_2)^m, \tag{3.6}$$

where Γ_1 and Γ_2 are the reflection coefficients at the terminal and fault location, respectively. The reflection coefficients are given by

$$\Gamma_1 = \frac{Z_1 - Z_0}{Z_1 + Z_0}, \quad \Gamma_2 = -1, \tag{3.7}$$

$$Z_1 = sL_{\text{cb}} + Z_{\text{CON}} // Z_2, \tag{3.8}$$

where Z_{CON} and Z_2 represent the equivalent impedance of the converter and the adjacent cables, respectively, as illustrated in Fig. 3.2. Although the transfer function of the subsequent waves with the reflection coefficients in frequency domain can be written directly, it is not trivial to derive the analytical expressions in time-domain, especially for meshed DC grids. To analyze the transient performance of the system, time-domain estimation of the traveling waves is necessary.

3.3.2 Time-domain Estimation of Traveling Waves

As shown in Fig. 3.2, a pole-to-pole fault occurs on $Line_{i1}$ connected to terminal (Bus_i) of the MTDC grid. The time-domain expression for the surge voltage traveling towards Bus_i can be attained by solving (3.5) as [57]:

$$v_1(z,t) = V_0 \cdot \text{erfc}(\frac{K}{4L\sqrt{t-z/c}} \cdot \frac{z}{c}) \cdot u(t-\frac{z}{c}), \tag{3.9}$$

where $u(t)$ is a step function and $\text{erfc}(t)$ is the complementary error function.

The equivalent circuit for the traveling wave at the terminal of $Line_{i1}$ is shown in Fig. 3.4(a), where u_q is the incident wave arriving at the terminal before the CB. Based on Peterson's rule, u_q is doubled and set as the voltage source in equivalent circuit of Fig. 3.4(a). The equivalent circuit is composed of the parallel branches connected to Bus_i. The cable $Line_{ij}$ is represented by its characteristic impedance Z_0, with the limiting reactor $L_{\text{cb,ij}}$ in series with the DC CB on this line. Subsequent to a fault occurrence, the converter is not immediately blocked and can be represented by an R-L-C branch [58]. The reflection coefficient at the terminal of the faulty cable Γ_1 can be estimated in time domain by

$$\begin{aligned} \Gamma_1 &= \frac{u_\text{f}}{u_\text{q}} = \frac{u_\text{t}}{u_\text{q}} - 1, \\ u_\text{t} &= u_\text{q} - Z_0 \cdot i_{\text{f,1}}, \end{aligned} \tag{3.10}$$

where, u_q is the first incident voltage arriving at the terminal with the time-domain expression described in (3.9), u_f is the reflected backward voltage and u_t is the refracted voltage transmitted into the terminal. The fault current $i_{\text{f,1}}$ is contributed by the converter capacitance and the adjacent cables discharge, denoted as $i_{\text{f,CON}}$ and $i_{\text{f},j}$ respectively, yielding

$$i_{\text{f,1}} = i_{\text{f,CON}} + \sum_{j \notin \{1,i\}} i_{\text{f},j} = C_\text{CON} \frac{\text{d}u_{C_\text{CON}}}{\text{d}t} + \sum_{j \notin \{1,i\}} i_{\text{f},j}. \tag{3.11}$$

The differential equations governing the behavior of the equivalent circuit are expressed by

$$\begin{aligned} 2u_\text{q} &= Z_0 i_{\text{f,1}} + L_{\text{cb,i1}} \frac{\text{d}i_{\text{f,1}}}{\text{d}t} + u_\text{bus}, \\ u_\text{bus} &= Z_0 i_{\text{f},j} + L_{\text{cb,ij}} \frac{\text{d}i_{\text{f},j}}{\text{d}t} \\ &= L_\text{CON} \frac{\text{d}i_{\text{f,CON}}}{\text{d}t} + R_\text{CON} i_{\text{f,CON}} + u_{C_\text{CON}}, \end{aligned} \tag{3.12}$$

where u_bus represents the voltage at the busbar. Therefore, the reflection coefficient can be computed based on the solution of (3.12). As shown in Fig. 3.4(b), due to the increase of $i_{\text{f,1}}$, Γ_1 decreases over time, which can be fitted as a linear function of time. As the network remains the same, the approximate reflection coefficient is used for the rest of the waves. Consequently, the superposition of all the incident waves at the terminal of the faulty cable yields:

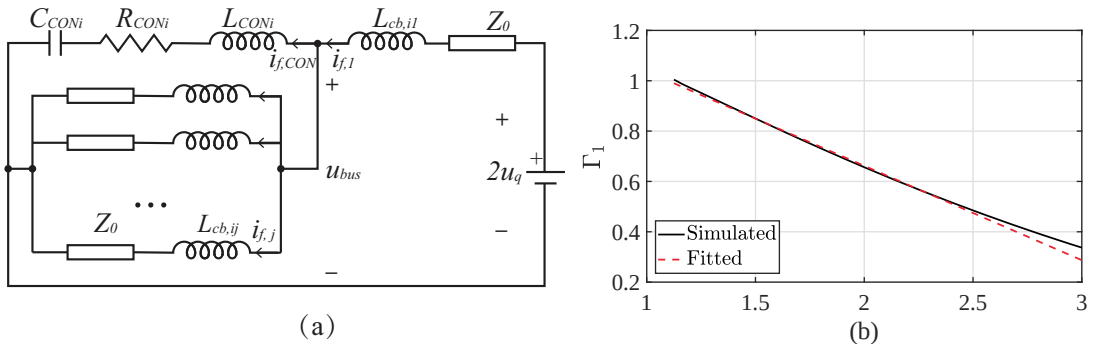

Figure 3.4: a) Equivalent DC circuit under a pole-to-pole fault; and b) the reflection coefficient at the terminal of the faulty cable.

$$u_{\mathrm{q}} = \sum_{m=0}^{\infty} u_{mq} = \sum_{m=0}^{\infty} v_1(l+2ml,t)(\Gamma_1\Gamma_2)^m. \tag{3.13}$$

Upon detection of a DC fault, the converter is blocked. The blocking signal generated by DESAT protection of the converter switches is faster than any other protective action. In this report, 1 ms is added to the signal of fault detection to represent the time delay in real system [59]. At the same time, the trigger signal for DC breaker is generated and the current starts to commutate to the main breaker. Then, after a delay, the main breaker opens to clear the DC fault. Based on the operation of DC breaker, the analysis and calculation are divided into three stages, and based on the state of the converter, the time interval before the main breaker opens can be subdivided into three stages, of which the equivalent model of converter are different. Based on the time-domain estimation of the traveling waves for the pole-to-pole fault at distance l from Bus_i on $Line_{i1}$, as shown in Fig. 3.2, the following transient response of the system during the fault clearance can be calculated by using the equivalent circuit at each stage, of which the maximum fault current and the maximum voltage can be determined.

Stage 1*: before the main breaker opens* ($t_0 \leq t \leq t_1$): The fault occurs at $t = 0$ and the first wave reaches the terminal of the faulty cable at $t = t_0$. Once the fault is detected and the trip signal is generated, the DC breaker starts to operate and the fault current is commutated from the LCS to the main breaker. Next the UFD opens. Subsequently, the main breaker opens after a delay t_{delay}, which is equal to the summation of the fault detection time and the turn-off time of NCP. Thus, the time at which the main breaker opens is $t_1 = t_0 + t_{\mathrm{delay}}$. The converter is blocked when the fault is detected. Thus, this stage can be divided into the followings:

A) discharging ($t_0 \leq t \leq t_{b1}$): As the fault detection delay is t_{detect}, the blocking time of the converter is $t_{\mathrm{b1}} = t_0 + t_{\mathrm{detect}}$. The equivalent circuit of this stage is the same as the one shown in Fig. 3.4(a). The only difference is in the value of u_{q}. Instead of using only the first incident wave, all subsequent waves are considered in Stage 1. The superposition of these waves is calculated in (3.13). Prior to blocking, the discharging of the capacitors in the converter contributes to the fault current, which is modeled as an equivalent R-L-C circuit.

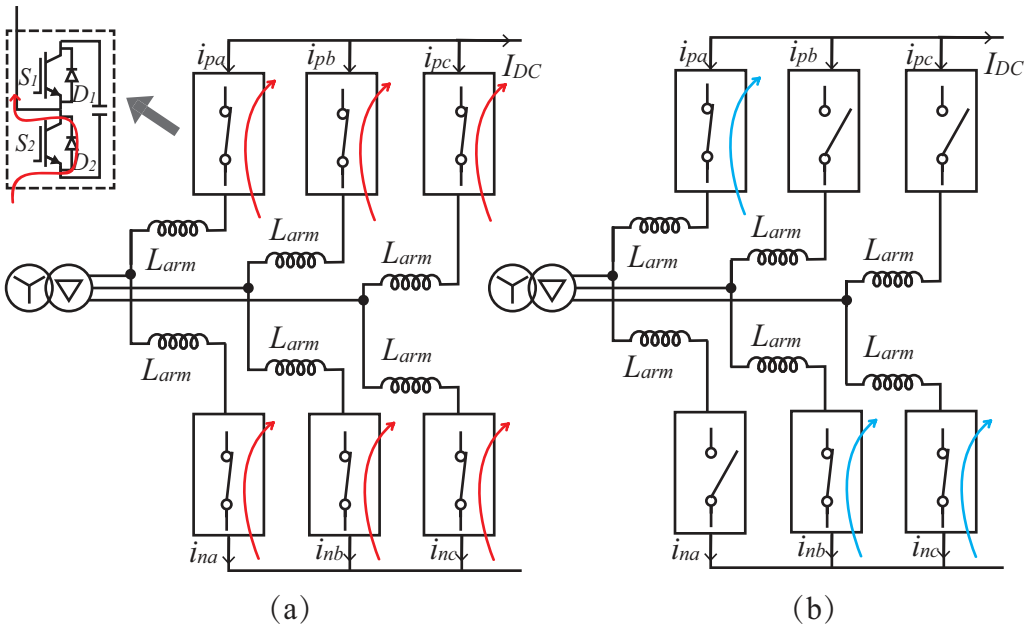

Figure 3.5: Conducting arms of the MMC: a) Stage 1B and b) Stage 1C.

B) diode free wheeling ($t_{b1} \leq t \leq t_{b2}$): The DC components of the arm currents increase rapidly in the discharging stage. The arm currents are all below zero at the time the IGBTs are blocked, so the current flows through diode D_2 in each submodule and starts to decrease, as shown in Fig. 3.5(a). This stage continues until current zero crossing occurs in any arm of the converter. The DC voltage of the converter can be equal to zero while the AC side contributions are balanced and sum to zero. In each arm, the arm current contains an increasing AC component and a decreasing DC component, which is used to determine the end of this stage. The equivalent circuit in this stage is shown in Fig. 3.7(a), where $U_{\text{con}i} = 0$.

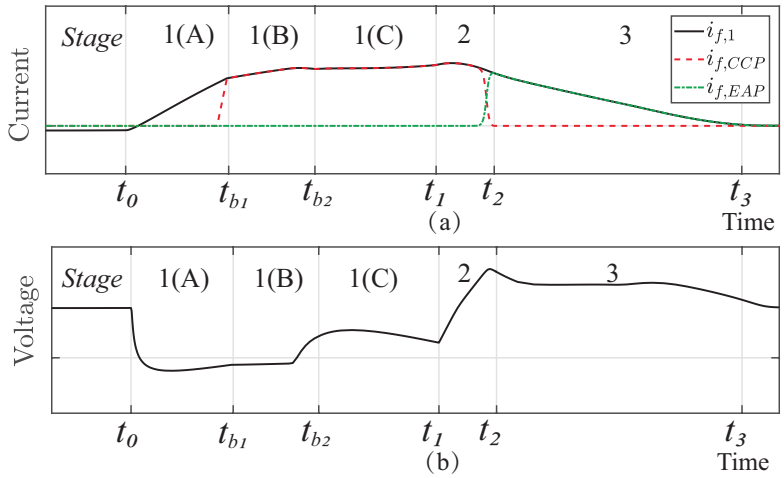

Figure 3.6: The waveforms during DC breaker operation: a) current on each branch of DC CB and b) bus-side voltage of DC CB.

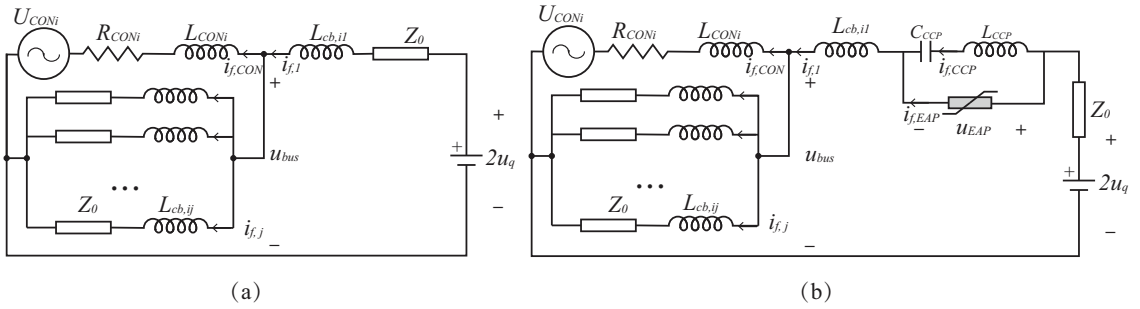

Figure 3.7: Equivalent DC circuits of a pole-to-pole fault: a) Stages 1B and 1C; and b) Stage 2.

C) diode rectifier ($t_{b2} \leq t \leq t_1$): At this stage, as shown in Fig. 3.5(b), three arms are conducting from the upper and lower arms of different phases. Thus, by converting this connection of the three phases of the AC voltages, the converter becomes equivalent to a voltage source. To simplify the calculation, the same equivalent circuit as in Stage 1B can be applied, where

$$U_{\mathrm{CON}i} = \frac{3}{2} U_{\mathrm{maxp}}, \tag{3.14}$$

where U_{maxp} is the peak phase-to-neutral voltage. The converter is blocked until the fault is isolated, thus the model of the converter stays the same in the following stages. During this stage, fault current continues to increase until the main breaker opens at $t = t_1$, so the maximum current $I_{\max}$ can be obtained based on the solution of (3.11) and (3.15).

$$\begin{aligned} 2u_{\mathrm{q}} &= Z_0 i_{\mathrm{f},1} + L_{\mathrm{cb,i1}} \frac{\mathrm{d}i_{\mathrm{f},1}}{\mathrm{d}t} + u_{\mathrm{bus}}, \\ u_{\mathrm{bus}} &= Z_0 i_{\mathrm{f},j} + L_{\mathrm{cb,ij}} \frac{\mathrm{d}i_{\mathrm{f},j}}{\mathrm{d}t} = L_{\mathrm{CON}} \frac{\mathrm{d}i_{\mathrm{f,CON}}}{\mathrm{d}t} + R_{\mathrm{CON}} i_{\mathrm{f,CON}} + U_{\mathrm{CON}i}. \end{aligned} \tag{3.15}$$

The fault current $i_{\mathrm{f},1}$ and bus-side voltage v_{ca} during DC breaker operation in Stage 1 are shown in Fig. 3.6. As shown, the bus-side voltage of DC breaker drops below zero at t_0 and the fault current $i_{\mathrm{f},1}$ continues to increase until the main breaker opens at $t = t_1$. The increase rate of the fault current becomes much lower when the converter is blocked at t_{b1}, as shown in Fig. 3.6(a).

***Stage 2**: current commutation to the arrester ($t_1 \leq t \leq t_2$)*: When the main breaker is switched off at $t = t_1$, the transient voltage across the main breaker rapidly increases until the arrester starts to conduct and clamps the voltage. The fault current in the main breaker is forced to the arrester and finally reaches zero at $t = t_2$. As shown in Fig. 3.6, Stage 2 starts at $t = t_1$, i.e., the moment the main breaker opens. The current $i_{f,\mathrm{CCP}}$ decreases to zero and $i_{f,\mathrm{EAP}}$ increases rapidly when the voltage across the arrester reaches its rated voltage. The equivalent model of the DC breaker during Stage 2 is shown in Fig. 3.7(b). The main breaker is equal to an equivalent capacitor C_{CCP} and an equivalent inductance L_{CCP} when the IGBTs are switched off. The nonlinear V-I characteristics of the arrester can be expressed as the fitted curve by:

$$i_{\mathrm{f,EAP}} = k \cdot u_{\mathrm{EAP}}^{\alpha}, \tag{3.16}$$

where k and α are the constants of the arrester and the voltage u_{EAP} is equal to the voltage across

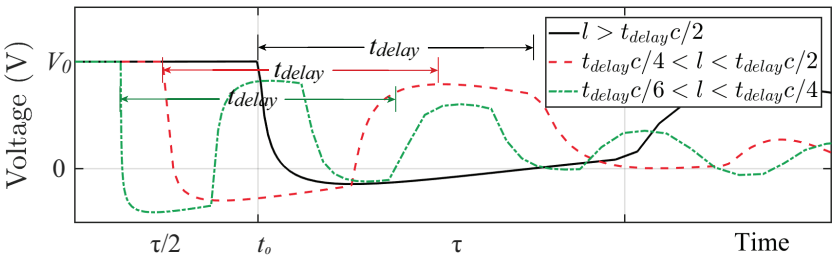

Figure 3.8: Voltage at the terminal of the faulty cable with different fault location.

the main breaker, which is charged by its current $i_{\mathrm{f,CCP}}$. Hence, the equations governing the breaker transient behavior are:

$$i_{\mathrm{f},1} = i_{\mathrm{f,CCP}} + i_{\mathrm{f,EAP}}, \tag{3.17a}$$

$$i_{\mathrm{f,CCP}} = C_{\mathrm{CCP}} \frac{\mathrm{d}u_{C_{\mathrm{CCP}}}}{\mathrm{d}t}, \tag{3.17b}$$

$$u_{\mathrm{EAP}} = L_{\mathrm{CCP}} \frac{\mathrm{d}i_{\mathrm{f,CCP}}}{\mathrm{d}t} + u_{\mathrm{CON}i}. \tag{3.17c}$$

KVL for the circuit of Fig. 3.7(b) yields

$$2u_q = u_{\mathrm{EAP}} + Z_0 i_{\mathrm{f},1} + L_{\mathrm{cb,i1}} \frac{\mathrm{d}i_{\mathrm{f},1}}{\mathrm{d}t} + u_{\mathrm{bus}}. \tag{3.18}$$

The elevation of voltage across the DC breaker also causes over voltage on the bus-side voltage of the breaker, of which the maximum voltage V_{max} occurs at the time the arrester starts to clamp the voltage, as shown in Fig. 3.6(b). By solving (3.16) to (3.18) in this stage, V_{max} can be found from the numerical solutions of the voltage.

***Stage 3**: fault current down to zero ($t_2 \leq t \leq t_3$)*: After the main breaker completely opens at $t = t_2$, the increase impedance of the arrester forces the DC fault current to rapidly decrease. As shown in Fig. 3.6, the bus-side voltage of DC breaker is clamped and the current $i_{f,\mathrm{EAP}}$ decreases until reaches zero at $t = t_3$, which is the end of the breaker operation. Thus, in Fig. 3.7(b), the equivalent circuit of the CCP is removed and only the arrester remains connected in the equivalent circuit during Stage 3. The currents and voltages during Stage 3 can be computed by the same method in Stage 2. The time from t_2 to t_3 is called the breaking time, t_{breaking}, of the DC breaker. The operation time of the DC breaker, defined as t_{clear}, is from t_0 to t_3. Subsequently, the energy absorbed by the arrester, W_{EAP}, can be computed by

$$W_{\mathrm{EAP}} = \int_{t_0}^{t_3} u_{\mathrm{EAP},i} i_{\mathrm{f,EAP}} \mathrm{d}t. \tag{3.19}$$

3.3.3 Estimation of the Worst-case Fault Location

Based on the aforementioned time-domain analysis, I_{max}, V_{max}, t_{clear} and W_{EAP} can be obtained from the numerical solutions for the fault at distance l from the terminal, which are taken as the

metrics for optimum selection of the DC breaker parameters. Since the fault can happen anywhere on the cable and the distance of the fault location has an impact on $I_{\max}$, $V_{\max}$, t_{clear} and W_{EAP}, it is necessary to indicate the fault location for the worst case scenario with maximum $I_{\max}$ and $V_{\max}$. The worst-case fault location problem has been investigated in [60] [61]. However, the relationships between fault location and fault metrics have not yet been analyzed. Additionally, the worst-case distances of the transmission lines that are shorter than the critical distance are not calculated. The following analysis fills this gap and provides a guidance for the optimal selection of system parameters.

For pole-to-pole faults at different distance l, the waveforms of the voltage at the terminal of the faulty cable are shown in Fig. 3.8. As shown, several reflections result in several voltage peaks. The duration of each reflection is $\tau = 2l/c$. The increase rate of fault current depends on the voltage across L_{cb}. If the voltage wave u_{q} is at the lower peak, the increased voltage across L_{cb} results in a higher rate of increase of the fault current. On the contrary, during the duration of u_{q} at the higher peak, the fault current increases slowly due to the reduced voltage difference across L_{cb}.

The maximum current within the time interval t_{delay} changes with the fault location. The relationship between the maximum current $I_{\max}$ and l is as follows:

- If $l > t_{\text{delay}}c/2$, which corresponds to $t_{\text{delay}} < \tau$, the increase rate of the fault current is at a high level. Considering the attenuation of the propagation wave, a lower distance l results in a higher di/dt and subsequently a larger $I_{\max}$. Thus, the worst fault location with maximum current is when $\tau = t_{\text{delay}}$. This location, which is $l_0 = t_{\text{delay}}c/2$, is defined as the characteristic length.
- If $t_{\text{delay}}c/4 < l < t_{\text{delay}}c/2$, which corresponds to $\tau < t_{\text{delay}} < 2\tau$, there will be an interval in which the current increases slowly and the duration of this interval increases with l. Therefore, as l increases, $I_{\max}$ decreases.
- When the fault is located closer to the terminal in the next interval, as mentioned earlier, the longer the duration of the lower peak of the wave u_{q} is, the higher $I_{\max}$ is. If the fault location is too close to the terminal, τ becomes much less than t_{delay} and the time interval with higher increase rate can be regarded as equal to half of t_{delay}. Hence, $I_{\max}$ increases with shorter l due to the attenuation of u_{q}.

Furthermore, at a fault location with a larger maximum current, when the main breaker opens, the next increasing reflection adds to the voltage generated by the breaker, causing a higher maximum overvoltage. The relationship between the maximum voltage $V_{\max}$ and l is similar to $I_{\max}$. For optimum parameter selection, $I_{\max}$ and $V_{\max}$ should be calculated for the worst case scenario, which is when the fault occurs at the defined characteristic location l_0 on the faulty cable. In addition, if the length of the cable is lower than l_0, the fault location should be given by comparing the possible peak values.

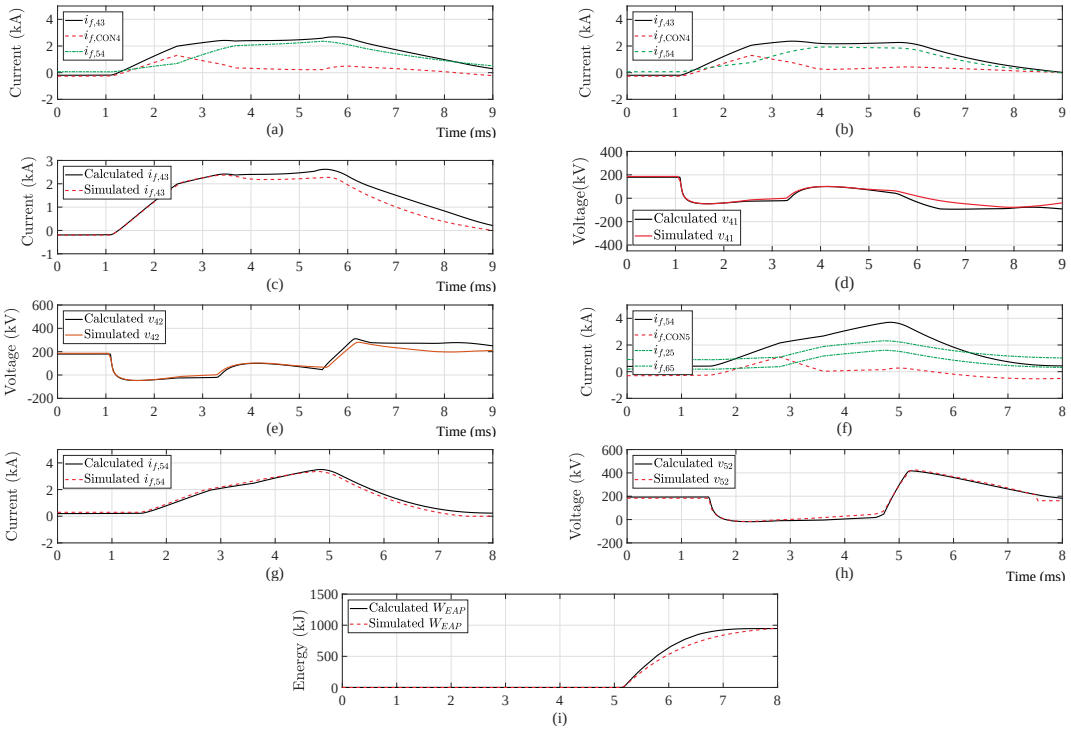

Figure 3.9: Calculated and simulated results: Case 1: a) calculated currents; b) simulated currents; c) fault current $i_{f,43}$; d) cable-side voltage v_{41}; and e) the bus-side voltage v_{42}; Case 2: f) calculated currents; g) fault current $i_{f,54}$; h) bus-side voltage v_{52}; and i) energy absorption W_{EAP}.

3.4 Parameter Optimization

The maximum current and voltage, clearing time, and as well as energy absorption in arresters are critical in system protection and fast recovery from DC faults. These metrics are influenced by the parameters of the DC breaker components, which should be optimally selected when designing the system. Among all the parameters of the DC circuit breaker, the current limiting reactor, the rated voltage of the arrester and the delay time are of the most critical factors influencing the breaker performance. The current limiting reactor is used to limit the maximum current within the interruption capability of the DC breaker. The rated voltage of the arrester determines the overvoltage level and the decrease rate of the fault current directly. The delay time, which is limited by the opening speed of the UFD, is always one of the most important determinants of the operation time of the DC breaker.

Due to the different influence of each parameter on the transient response, it is difficult to select an optimal combination of them. The series-connected current limiting reactor of the DC breaker can limit the increase rate of fault current. However, it ironically impacts the maximum voltage by increasing the reflection coefficient and lengthening the interruption time of the CB. In addition, the reactors in the adjacent cables can also influence the overcurrent and overvoltage. The increase of the delay time for the UFD before the main breaker opens, can increase the maximum current. However, the maximum voltage also depends on the traveling wave during the time delay. Furthermore, reducing the rated voltage of the arrester can reduce the overvoltage to a lower level.

However, it will lengthen the operation time of the breaker.

Therefore, all the trade-offs among $I_{\max}$, $V_{\max}$, t_{clear} and W_{EAP} should be taken into the optimization, which requires help of quantitative calculation. In this report, the proposed time-domain method for transient response and the genetic algorithm are used to solve the optimization problem. The process includes the followings:

- Based on the detailed analysis during the fault clearance process presented in Section III, $I_{\max}$, $V_{\max}$, t_{clear} and W_{EAP} can be obtained from the numerical solutions. $I_{\max}$, $V_{\max}$, t_{clear} and W_{EAP} are nonlinear functions of the parameters $L_{\text{cb,i1}}...L_{\text{cb,ij}}$, t_{delay} and U_{r}, which can be expressed by

$$f_m(x), m = 1,2,3,4; \tag{3.20a}$$
$$x = [L_{cb,i1}...L_{cb,ij}, t_{delay}, U_r]; \tag{3.20b}$$
$$I_{max} = f_1(x); \tag{3.20c}$$
$$V_{max} = f_2(x); \tag{3.20d}$$
$$t_{clear} = f_3(x); \tag{3.20e}$$
$$W_{\text{EAP}} = f_4(x); \tag{3.20f}$$

  where $L_{\text{cb,i1}}...L_{\text{cb,ij}}$ represent the reactors in the faulty cable and the adjacent cables. In the practical MTDC systems, the reactors of different lines might be different and need to be optimized independently at the same time.

- The bound of each parameter is based on the voltage class and rated power of the system. These bounds, which are determined by the cost, insulation coordination, etc., can be obtained from the specifications of a real system. The current limiting reactor should be large enough to limit the maximum current within the interruption capability of the DC breaker. However, it is constrained by the cost and volume. The range of the rated voltage of the arrester is based on the insulation level of the DC lines. The delay time of the DC breaker is mainly limited by the opening speed and the voltage withstanding capability of the UFD.

- The multi-objective problem, which aims to minimize the $I_{\max}$, $V_{\max}$, t_{clear} and W_{EAP} by optimal selection of the parameters within their bounds, can be formulated as

$$\underset{x}{\text{minimize}} \quad f_m(x) \tag{3.21a}$$
$$\text{subject to} \quad W_{EAP,1} = W_{EAP,2} = ...W_{EAP,N}, \tag{3.21b}$$
$$x_i^L \le x_i \le x_i^U, i = 1,2,...,n. \tag{3.21c}$$

  where $x = [L_{\text{cb,i1}}...L_{\text{cb,ij}}, t_{\text{delay}}, U_{\text{r}}]$, and $f_m(x)$ represents the metrics $I_{\max}$, $V_{\max}$, t_{clear} and W_{EAP} with respect to the variables $L_{\text{cb}}, t_{\text{delay}}$ and U_{r}. In addition, for the sake of convenience

for computation, it is assumed that all the reactors are identical and denoted by L_{cb} in this report. The genetic algorithm is then applied to compute Pareto-optimal sets for (3.21).

- By the genetic algorithm, a set of solutions of this multi-objective problem can be obtained with the corresponding metrics. Although the metrics are not minimized at the same time, the optimal parameters can be selected from the solutions according to the requirements of the system protection. Some of the metrics can be the minimum while others are limited within their specified ranges.

3.5 Study Results

In this section, the MMC-MTDC system of Fig. 3.1 is built in the PSCAD/EMTDC software environment for time-domain simulations with frequency-dependent, distributed cable model. To evaluate the degree of accuracy and examine the validity of the calculations based on the equivalent circuits, the calculation results are compared with the corresponding results obtained from the exact model of the study system in the PSCAD. The main parameters of the system are listed in Table 3.1. The distributed parameters of the cable used in the calculations are from the PSCAD Line Constants Program at the frequency of 0.1 MHz [49], which is based on the fact that the high frequency range of propagation matrix quantities are almost constant. Considering the skin effect at high frequency, the characteristic impedance is $Z_0 = \sqrt{(sL + K\sqrt{s})/(sC)} \approx \sqrt{L/C}$. The skin effect factor $K = R_{HF}/\sqrt{\pi \cdot f_{HF}}$.

Table 3.1: Converter and grid parameters,

	Conv. 1	Conv. 2-5
Rated capacity [MVA]	450	120
Rated DC Voltage [kV]	± 200	± 200
Rated AC voltage [kV]	220	220
Operation Mode Setpoints	± 200 [kV]	-100 [MW]

3.5.1 Evaluation of the Transient Analysis

Case 1: The positive and negative poles are shorted at a distance of 200 km from Bus_4 on $Line_{34}$. The breakers CB_{43} and CB_{34} operate once the trip signals are generated. In this case, the current limiting reactors L_{cb} are equal to 100 mH and t_{delay} is set at 4 ms. The switching voltage of the breaker is usually designed from 1.2 pu to 1.5 pu with considering fast current interruption and insulation level [45] [52]. Therefore, the rated voltage of arresters in DC breakers is set at 300 kV. The fault current $i_{f,43}$, the current contributed from the converter $i_{f,CON4}$ and the current from the adjacent cable $i_{f,54}$ are measured in the simulation. The cable-side and the bus-side voltages of the DC breaker are also recorded as v_{41} and v_{42}, respectively.

The waveforms of the corresponding current and voltage from calculation based on the equivalent circuit model are compared with the simulation results in Fig. 3.9. The fault occurs at $t = 0$ ms

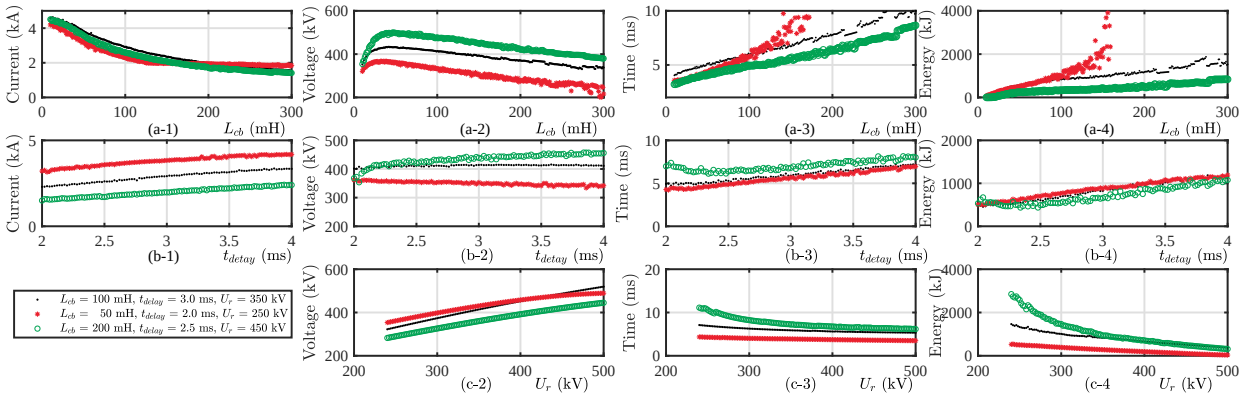

Figure 3.10: Calculated results for $I_{\max}$, $V_{\max}$, t_{clear} and W_{EAP} with one parameter being changed: (a-1)-(a-4) objectives vary with L_{cb}; (b-1)-(b-4) objectives vary with t_{delay}; and (c-1)-(c-3) objectives vary with U_{r}.

and reaches the terminal at $t = 1.08$ ms. The fault current through the DC breaker increases very fast. Based on the computed and the simulated currents shown in Figs. 3.9(a) and (b), the current of the faulty cable is contributed by the converter and the adjacent cable. The increase rate at the first stage, which is determined by the voltage across L_{cb}, is quite high because the voltage at the cable side of the breaker, v_{41}, drops below zero due to the first reflection at the terminal, shown in Fig. 3.9(d). When the converter is blocked at $t = 2.53$ ms, the increase rate is much lower due to the decrease of current from converter. During the next stage, on one hand, the equivalent voltage source of the converter contributes to the increase of the fault current. On the other hand, the voltage v_{42} at the second reflection limits its increase rate. Therefore, the fault current does not increase any longer during this interval and reaches its maximum value at the end of the first reflection at $t = 3.24$ ms. At $t = 5.53$ ms, the main breaker opens and the voltage across it rises very fast because of the restored energy in the inductance of the DC circuit. Consequently, as shown in Fig. 3.9(e), the voltage at the bus side of DC breaker v_{42} increases as well until the arrester clamps the voltage. The maximum voltage is mainly based on the rated voltage of the arrester U_{r}. The voltage v_{41} at its second reflection can also increase the maximum voltage of v_{42}. In this stage, the counter voltage forces the fault current to decrease until it reaches zero. So, a higher U_{r} causes a higher maximum voltage and a larger decrease rate of current, thereby reducing the fault clearance time.

Figs. 3.9(c)-(e) show a close agreement between the exact response obtained from the PSCAD / EMTDC model and that of the calculated one from the equivalent circuit. Since the computation is based on the high-frequency model, the differences with the simulation occur at the later stage of the wavefront. Consequently, the maximum current and the maximum voltage are slightly larger than the simulated ones. However, in view of the safety margin of fault protection, this is acceptable in the parameter optimization algorithm.

Case 2: The objective of this case, performed at Bus_5 with three cables connected in parallel, is to examine the applicability of the calculation method to several adjacent cables in a complex network. In this case, L_{cb}=100 mH and the delay time t_{delay}=3 ms, so the worst case is taken with a pole-to-pole fault at 275 km, i.e., the characteristics length l_0, from Bus_5 at $Line_{45}$.

The comparison of the calculated and simulated results is shown in Fig. 3.9. Based on the currents from calculation and simulation shown in Figs. 3.9(f) and (g), respectively, the fault current $i_{f,54}$ is the summation of the currents from converter and the adjacent cables. The increase rates of the current from adjacent cables, $i_{f,25}$ and $i_{f,65}$, are the same due to the same L_{cb} and Z_0. Prior to opening the main breaker, the cable-side voltage of the breaker v_{51} is mainly at the first reflection. Thus, the fault current $i_{f,54}$ keeps increasing fast in this interval, except the duration with lower increase rate at the stage after converter blocking, because of the large voltage difference across L_{cb}. At the moment the main breaker opens at $t = 4.75\,\text{ms}$, voltage v_{51} starts to increase at its second reflection. Therefore, the voltage on the bus side of DC breaker v_{52} equals to the superposition of v_{51} and the voltage across the DC breaker, resulting in the most severe overvoltage of v_{52}. This confirms that not only the limiting reactor and the rated voltage of the arrester impact the transients, but also the delay time before main breaker opens, influences the maximum current and the maximum voltage, which determines the fault location of the worst case and the increasing time of fault current. At the moment when the voltage across the main breaker reaches the rated voltage, the arrester starts to conduct and absorb the residual energy, as shown in Fig. 3.9(i).

3.5.2 Optimum Parameter Selection of the Breaker

As demonstrated earlier, the parameters of the system and the DC breaker have significant impacts on the transient performance during the fault clearance. The current limiting reactor L_{cb}, the delay time of the breaker t_{delay} and the rated voltage U_r are taken as the parameters to be optimized in this report. With the algorithm shown in Section III, the objectives including the maximum current I_{max}, the maximum voltage V_{max}, the operating time t_{clear} and the energy absorption W_{EAP} during breaker operation are written as functions of these variables. Based on the layout of Bus_4 in Case 1, three sets of parameters are chosen:

- $L_{cb} = 100\,\text{mH}$, $t_{delay} = 3.0\,\text{ms}$, $U_r = 350\,\text{kV}$.
- $L_{cb} = 50\,\text{mH}$, $t_{delay} = 2.0\,\text{ms}$, $U_r = 250\,\text{kV}$.
- $L_{cb} = 200\,\text{mH}$, $t_{delay} = 2.5\,\text{ms}$, $U_r = 450\,\text{kV}$.

For each set of parameters, calculations for I_{max}, V_{max}, t_{clear} and W_{EAP} are made by changing one variable. The relationship between the objectives with each variable is analyzed with the results shown in Fig. 3.10.

As shown in Fig. 3.10(a-1), by increasing L_{cb}, the increase rate of the fault current and consequently the maximum current is reduced. Due to the increase of L_{cb}, on one hand, the voltage generated by the reactor to limit the current increases. On the other hand, the larger L_{cb} causes a larger reflection coefficient, resulting in a lower voltage at the terminal. Consequently, as shown in Fig. 3.10(a-2), with the increase of L_{cb}, the maximum voltage first increases and then decreases. The operation time increases due to the reduced decrease rate of current with a larger L_{cb} after the main breaker opens, as demonstrated in Fig. 3.10(a-3). The energy absorption, shown in Fig. 3.10(a-4), increases with the increase of L_{cb} when L_{cb} is lower than 100 mH. As the red curve shown in Figs. 3.10(a-3) and 3.10(a-4), the fault is hard to clear when the reactor is too large

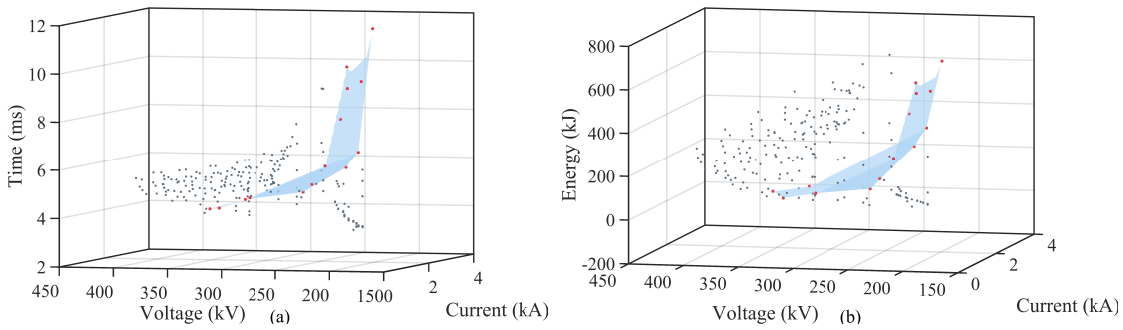

Figure 3.11: Pareto-optimal front of the feasible objective space.

with a much lower U_r. It is shown in Fig. 3.10(b-1) that a longer t_{delay} provides a longer time for increase of current, which results in a larger I_{max}. When the delay time increases, the characteristic length l_0 increases and the attenuation of the surge voltage decreases the voltage drop after the fault. Thus, V_{max} shown in Fig. 3.10(b-2) increases with the increase of t_{delay}. The increase is more pronounced when t_{delay} is lower because the surge voltage attenuates faster at a closer distance. The operation time in Fig. 3.10(b-3) shows that a longer t_{delay} results in a longer t_{clear}. Also, the energy absorption W_{EAP} increases with the increase of t_{delay}. Although increase of U_r does not have a significant impact on I_{max}, it directly increases V_{max} and reduces t_{clear} and W_{EAP}, as shown in Figs. 3.10(c-1), (c-2) and (c-3).

Table 3.2: Selected parameters for optimized objectives.

	Parameters			Objectives			
	L_{cb} [mH]	t_{delay} [ms]	U_{r} [kV]	I_{max} [kA]	V_{max} [kV]	t_{clear} [ms]	W_{EAP} [kJ]
Case 1	100	3.0	300	2.30	353	6.12	352
Scheme 1	180	2.5	260	1.67	310	8.80	488
Scheme 2	135	2.6	410	1.92	397	5.85	143
Scheme 3	150	2.5	330	1.83	360	6.30	304

All the aforementioned trade-offs are considered in the multi-objective optimization problem described in Section IV, where L_{cb} is varied within a range from 1 mH to 200 mH, t_{delay} is varied from 2.5 ms to 3.5 ms and U_{r} is varied from 240 kV to 450 kV. With the variable ranges, the feasible objective space consists of the corresponding objectives is shown in Fig. 3.11. The trade-offs among the four objectives are revealed from the three dimensional graphs in Fig. 3.11. I_{max} and V_{max} are relatively independent of each other, while the increase of I_{max} or V_{max} will increase t_{clear} and W_{EAP}. By solving the multi-objective optimization problem, the best trade-off among the objectives is explored. In this report, this problem is solved with genetic algorithms and the solutions are shown by the red points in Fig. 3.11. The solutions composing a curved surface to the boundary of the objective space is the Pareto-optimal front, on which the points have optimized objectives. The corresponding variables provide optimal combinations of parameters for DC breakers. From the solutions, the DC CB can be designed in coordination with other factors in a real system. Three sets of parameters are chosen from the solutions and listed in Table 3.2 to show the improved transients. The transient performance of the system with the optimized parameters is tested by simulations.

$I_{\max}$, $V_{\max}$, t_{clear} and W_{EAP} with the selected parameters are compared with the worst case at Bus_4 with the same parameters as Case 1. Compared to the case before optimization, as shown in Table 3.2, the objectives with optimal parameters are reduced to a certain extent. In Scheme 1, $I_{\max}$ and $V_{\max}$ are much lower while in Scheme 2, $I_{\max}$, t_{clear} and W_{EAP} are reduced. Moreover, Scheme 3 reduces $I_{\max}$ and W_{EAP} while avoiding the increase of $V_{\max}$ and t_{clear}. Although the four objectives are not minimized simultaneously due to the trade-off, it would be ideal if they are limited within their specified ranges.

3.6 Conclusion

In this report, parameters of the hybrid solid state DC CB are optimally selected based on analytical calculation of the four metrics, i.e., maximum voltage, maximum current, operation time and absorbed energy during a pole-to-pole fault in an MTDC grid. To this end, a time-domain method is proposed to calculate the fault transient response during the DC breaker operation with considering all generated travelling waves. Accuracy and effectiveness of the proposed method are evaluated and verified by time-domain simulation studies in the PSCAD/EMTDC environment. Based on the proposed algorithm, the relationship between the fault performance metrics and the three parameters of the breaker, i.e., current limiting reactor, arrester rated voltage, and time delay are obtained from the numerical computation, which are all nonlinear functions of the parameters. By formulating a multi-objective optimization problem, the Pareto-fronts are explored to select the breaker parameters. The proposed method provides a systematic method to determine the best combination of DC CB parameters such that the maximum values of overcurrent and overvoltage imposed by the fault as well as the fault clearance time and energy absorption will stay within their specified limits.

4. Model Predictive Control-Based AC Line Overload Alleviation in Meshed AC/MTDC Grids

4.1 Introduction

High voltage DC (HVDC) transmission is a mature technology for transferring bulk power over long distances. Over the past few years, significant breakthroughs in Voltage Sourced Converters (VSCs) have made the HVDC technology a front-runner solution to reduce the cost and power losses, and to provide enhanced reliability and functionality. At the same time, significant changes in generation, transmission, and loads such as the integration of renewable, the retirement of numerous coal plants, and the need to supply the increasing power demands of cities have emerged [62]. These new trends have called for Multi-Terminal DC (MTDC) systems, which when embedded inside the AC grid, can enhance overall grid stability, reliability, and efficiency [63]. The MTDC grid can support the future AC grid by improving its frequency response of the AC grid [64–66], inter-area oscillation damping [67, 68], and reducing the operational cost of the electricity grid [69, 70]. In addition to the aforementioned functions, a MTDC grid can play a major role in AC line overload alleviation.

An AC line overload can cause line sag and even cascade tripping. Real-time system security level control of the grid usually takes place using a Security-Constrained Optimal Power Flow (SCOPF), which ensures that the impact of possible N-1 contingency overloads are taken into consideration in the dispatch. SCOPF with corrective actions has been proposed, which considers corrective actions for some critical AC line overloads [71]. This means that if a line gets overloaded, the operator takes predetermined control actions. SCOPF with corrective actions is inherently an open-loop method, which highly depends on the accuracy of the power system model. Among other open-loop methods, reference [72] proposes an optimal power flow that mitigates the AC line overloads. In [73], an algorithm is proposed to divide the grid into sub-grids such that power shift between the sub-grids mitigates the AC line overloads.

Over the past few years, closed-loop methods are becoming more prevalent, as they are more reliable and less model dependent. In [74], a Model Predictive Control (MPC)-based strategy is proposed, which controls the AC generators to alleviate AC lines overloads. This method is further investigated in presence of energy storage and renewable energy resources [75]. An online overload alleviation strategy based on linear programming is proposed in [76]. In all of the closed-loop strategies, the controller regularly receives measurements from the power system to assess its condition and modify the control inputs to direct the system to a secure state. To the best of our knowledge, in none of the existing closed-loop methods, a MTDC grid has been exploited as a control asset for any AC line overload alleviation. A salient advantage of a MTDC converter station over an AC generator is that its power change is not limited by a ramp rate limit. Furthermore, compared to the phase shifting transformers, it is fully controllable.

The contribution of this report is a MPC-based strategy, which uses MTDC converter stations along with the AC grid generators for transmission line overload alleviation. The objective is to reduce active powers of the overloaded AC lines by deploying the MTDC converters and AC generators. The advantage of the proposed controller is to simultaneously use the MTDC converter stations and AC system generators to relieve the overloads of AC lines. The proposed controller is integrated with the conventional Automatic Generation Control (AGC), thereby following a contingency, the system regulates frequency and mitigates AC line overloads, simultaneously. The controller receives the measurements within regular sampling time periods. When an outage imposes overloads on AC lines, the controller computes and dispatches the optimum setpoints of the active powers of the MTDC converters and the AC grid generators within each sampling time period. The optimum setpoints are computed by a MPC strategy to bring the active powers of the overloaded AC lines below their limits. To implement the MPC strategy, the sensitivity matrices relating the AC line active powers, DC line currents and DC bus voltages to the converters' active power setpoints and the generator active powers are calculated. Furthermore, all the operational constraints including constraints of the DC bus voltages, the DC line currents, the ratings of the MTDC converter stations, AC bus voltages, and the ramp rates are meticulously considered. The proposed controller constantly checks a voltage stability criterion to ensure that it does not push the system towards the voltage instability boundaries. The performance of the proposed controller is evaluated and demonstrated using time-domain simulation studies on two test systems, i.e., the 39-bus New England test system integrated with a 5-bus MTDC grid and the IEEE 118-bus test system integrated with a 6-bus MTDC grid.

4.2 The Proposed Method

With respect to Fig. 4.1, which indicates an example of a typical MTDC grid embedded within an AC grid, the well-known modular multilevel converters (MMCs) interconnect the AC buses to the DC buses. The controller of each onshore converter station regulates its reactive power to zero, while its real power is determined by either constant power mode or $P-V$ droop mode. The constant power mode implies that the power of each converter station is equal to the power setpoint, i.e., P_{MMC}^{ref}, which is computed by the controller proposed in this report. The active power of a converter station that uses $P-V$ droop mode is a linear function of its DC bus voltage as follows:

$$P_{MMC} = P_{MMC}^{ref} - k_v[V_{DC}^{ref} - V_{DC}], \tag{4.1}$$

where the reference of the DC bus voltage, i.e., V_{DC}^{ref} is constant and equal to 1 pu. Moreover, k_v and P_{MMC} represent the $P-V$ droop constant and the active power of the converter station injected to the AC grid, respectively.

Assuming that a large disturbance such as a line outage occurs at $t = 0$ s, the proposed controller receives the system measurements every $\Delta t = t_m$ s. The measurements are $\mathbf{P}_G^m$, $\mathbf{P}_L^m$, $\mathbf{I}_{DC}^m$, $\mathbf{P}_{MMC}^m$, and $\mathbf{V}_{DC}^m$, which are the vectors of the generator active powers, the AC line active powers, the DC line currents, the MTDC converter active powers, and the DC bus voltages, respectively. Following the outage, the controller sets the time interval T for AC line overload alleviation and the current

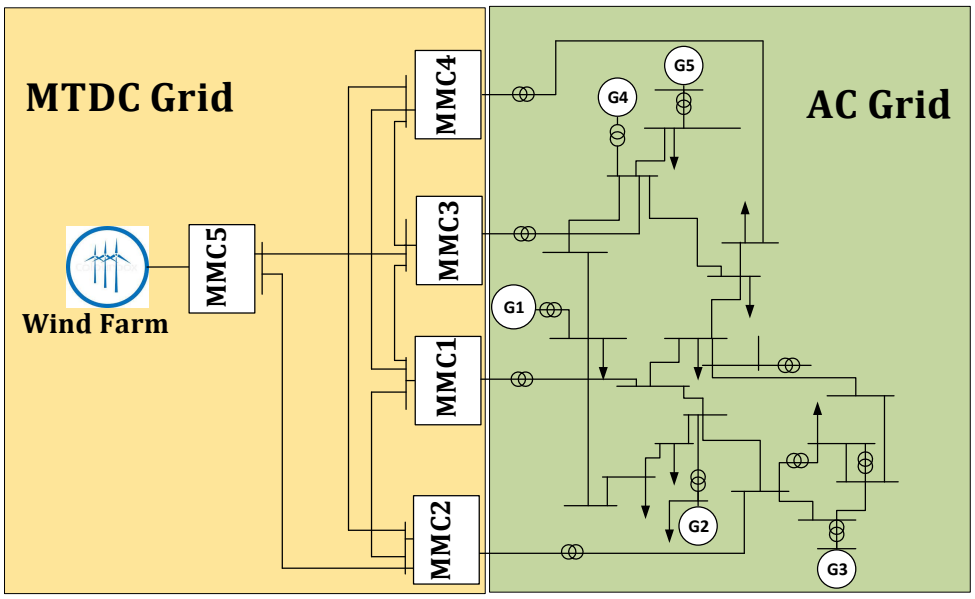

Figure 4.1: A typical MTDC grid embedded in an AC grid.

step to $k = 0$. As the controller receives the measurements, it calculates the optimum converters' active power setpoints, i.e., $\mathbf{P}_{MMC}^{ref}$ and the generator active powers, i.e., $\mathbf{P}_G$ for $k = 1, ..., c$, where, c is a predetermined control horizon. The prediction horizon is equal to the control horizon. The controller communicates $\mathbf{P}_{MMC}^{ref}$ and $\mathbf{P}_G$ to the MTDC converters and the AC system generators. Subsequently, the controller updates $k = k+1$ and repeats the same procedure until $t = T$ s. If the controller does not manage to mitigate all the AC line overloads in $t = T$ s, the system operator can reinitiate the controller. For example, if the operator expects the overload to reach below 80% of the rated power within $t = T$ s, but it reaches 85% of the rated power within that time interval, the operator can run the controller again.

The proposed control scheme is integrated with the conventional AGC and is shown in Fig. 4.2. As shown in Fig. 4.2, despite the fact that the converters' active power setpoints are only manipulated by the proposed controller, the generator active powers are influenced by both the AGC and the proposed controller. The implementation of the controller is detailed in the following.

Assume that subsequent to a contingency, the controller receives the k^{th} set of measurements at $t = k * t_m$ s. The control input vector is $\mathbf{u} = [\Delta\mathbf{P}_G, \Delta\mathbf{P}_{MMC}^{ref}]$. The controller must find the optimum control inputs for $k+1, k+2, ..., k+c$, which are shown by $\mathbf{u}(k+1), ..., \mathbf{u}(k+c)$, respectively. Moreover, the vectors of slack variables α and β are considered for the DC line currents and the AC line active powers, respectively. The j^{th} slack variable in α, which relaxes the corresponding AC line loading constraint is defined as

$$\alpha_j = \begin{cases} 0, & \text{if } P_{L(j)} \leq \gamma P_{L(j)}^{max} \\ P_{L(j)} - \gamma P_{L(j)}^{max}, & \text{if } \gamma P_{L(j)}^{max} < P_{L(j)} \end{cases} \tag{4.2}$$

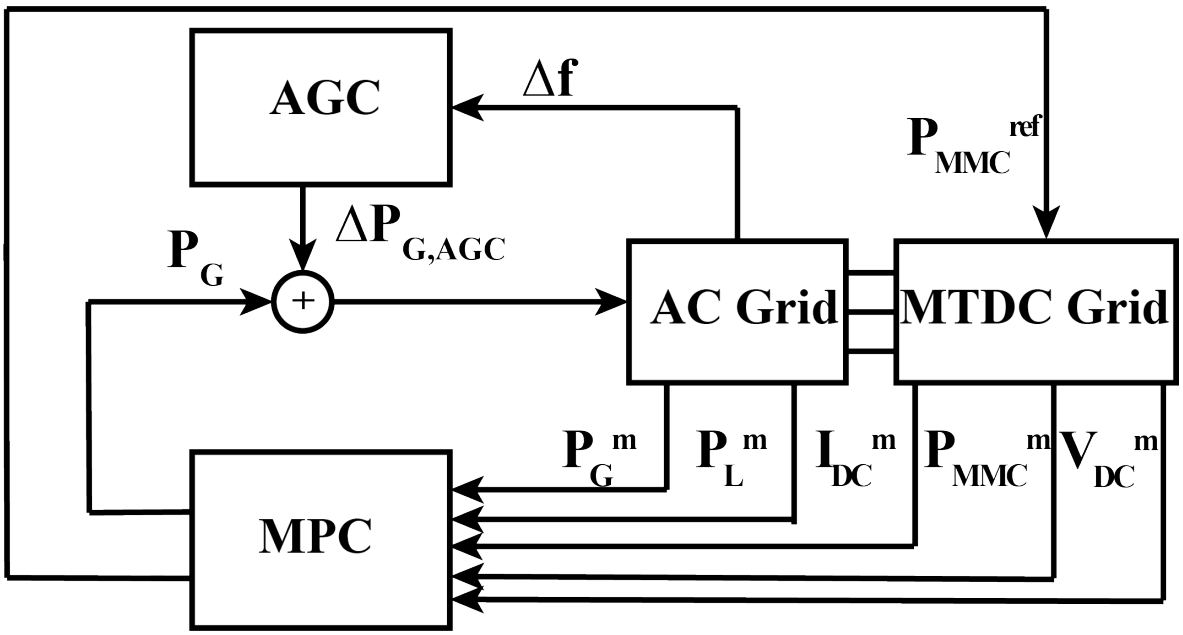

Figure 4.2: Overall block diagram representation of the proposed controller.

where $P_{L(j)}$ and $P_{L(j)}^{max}$ are the active power of the j^{th} AC line and the maximum power of the corresponding line, respectively. γ is a constant scalar, which is slightly greater than one and is considered to account for the case that the line is severely overloaded. Furthermore, the j^{th} slack variable in β, which relaxes the corresponding DC line loading constraint is defined as

$$\beta_j = \begin{cases} 0, & \text{if } I_{DC(j)} \leq I_{DC(j)}^{max} \\ I_{DC(j)} - I_{DC(j)}^{max}, & \text{if } I_{DC(j)}^{max} < I_{DC(j)}, \end{cases} \tag{4.3}$$

where $I_{DC(j)}$ and I_{DC}^{max} represent the current of the DC line and the corresponding maximum DC current, respectively. By embedding the slack variables in the the vector of control inputs, the vector of the decision variables for the controller is $\mathbf{z}_k = [\mathbf{u}(k+1)^T, \mathbf{u}(k+2)^T, ..., \mathbf{u}(k+c)^T, \alpha_k, \beta_k]$.

The MPC cost function is defined as

$$\begin{aligned} &\min_{\mathbf{P}_{MMC}^{ref}, \mathbf{P}_G, \alpha, \beta} \sum_{i=1}^{c} [\mathbf{P}_L^{target} - \mathbf{P}_L(k+i)]^T \mathbf{W}_L [\mathbf{P}_L^{target} - \mathbf{P}_L(k+i)] \\ &+ \sum_{i=1}^{c} [\Delta \mathbf{P}_G(k+i)]^T \mathbf{W}_G [\Delta \mathbf{P}_G(k+i)] \\ &+ \sum_{i=1}^{c} [\Delta \mathbf{P}_{MMC}^{ref}(k+i)]^T \mathbf{W}_{MMC} [\Delta \mathbf{P}_{MMC}^{ref}(k+i)] \\ &+ \sum_{i=1}^{c} \alpha(k+i)^T \rho_\alpha \alpha(k+i) + \sum_{i=1}^{c} \beta(k+i)^T \rho_\beta \beta(k+i), \end{aligned} \tag{4.4}$$

where $\mathbf{W}_L, \mathbf{W}_G$, and $\mathbf{W}_{MMC}$ are diagonal weighting matrices corresponding to the AC line active powers $\mathbf{P}_L$, the generator active power changes $\Delta \mathbf{P}_G$, and the converters' active power set-

point changes $\Delta \mathbf{P}_{MMC}^{ref}$, respectively, where, $\Delta \mathbf{P}_G(k+i) = \mathbf{P}_G(k+i) - \mathbf{P}_G(k)$ and $\Delta \mathbf{P}_{MMC}^{ref}(k+i) = \mathbf{P}_{MMC}^{ref}(k+i) - \mathbf{P}_{MMC}^{ref}(k)$ reflect the influence of the control input vectors in the cost function. $\mathbf{P}_L^{target}$ is the vector of the reference values for the AC line active powers. The assigned values for this reference vector will be shortly discussed. ρ_α and ρ_β are diagonal weighting matrices of the penalty functions to soften the constraints of the AC line active powers and the DC line currents, respectively. The first term in (4.4) is associated with the power flow of the AC lines, which should follow their reference values. Since it is impossible that the power flow of all the lines follow their corresponding reference values, different levels of overloads are defined. Hence, the more an AC line gets overloaded, a larger weighting factor is assigned to it. This helps the controller to force the lines that are highly overloaded to track their reference values. The second and third terms are considered to adjust the extent of MTDC grid participation in overload alleviation. If the diagonal entries of W_{MMC} are selected to be much smaller than the diagonal entries of W_G, the controller would use the MTDC converter stations as much as possible. The fourth and fifth terms are penalty functions, which will be shortly discussed.

The optimization problem in (4.4) is subjected to the following inequality constraints for $i = 1, 2, ..., c$:

- The AC system inequality constraints:

$$-\mathbf{R}_G^{max} \leq \mathbf{P}_G(k+i) - \mathbf{P}_G(k+i-1) \leq \mathbf{R}_G^{max}, \tag{4.5}$$

$$\mathbf{P}_G^{min} \leq \mathbf{P}_G(k+i) \leq \mathbf{P}_G^{max}, \tag{4.6}$$

$$-\gamma \mathbf{P}_L^{max} - \alpha(k+i) \leq \mathbf{P}_L(k+i) \leq \gamma \mathbf{P}_L^{max} + \alpha(k+i), \tag{4.7}$$

$$\mathbf{V}_{AC}^{min} \leq \mathbf{V}_{AC}(k+i) \leq \mathbf{V}_{AC}^{max}. \tag{4.8}$$

- The MTDC system inequality constraints:

$$-\mathbf{I}_{DC}^{max} - \beta(k+i) \leq \mathbf{I}_{DC}(k+i) \leq \mathbf{I}_{DC}^{max} + \beta(k+i), \tag{4.9}$$

$$\mathbf{V}_{DC}^{min} \leq \mathbf{V}_{DC}(k+i) \leq \mathbf{V}_{DC}^{max}, \tag{4.10}$$

$$-\mathbf{R}_{MMC}^{max} \leq \mathbf{P}_{MMC}^{ref}(k+i) - \mathbf{P}_{MMC}^{ref}(k+i-1) \leq \mathbf{R}_{MMC}^{max}, \tag{4.11}$$

$$-\mathbf{P}_{MMC}^{max} \leq \mathbf{P}_{MMC}(k+i) \leq \mathbf{P}_{MMC}^{max}, \tag{4.12}$$

where $\mathbf{I}_{DC}$ and $\mathbf{V}_{DC}$ represent the vectors of DC line currents and DC bus voltages of the MTDC system. $\mathbf{P}_{MMC}$ represents the vector of the converter active powers injected into the AC system. $\mathbf{P}_L$ is the vector of AC line active powers. $\mathbf{R}_G^{max}$ denotes the vector of ramp rate of all the AC system generators. $\mathbf{R}_{MMC}^{max}$ is the vector of maximum allowable change in the converters' active power setpoints. $\mathbf{P}_G^{max}$ and $\mathbf{P}_G^{min}$ are the vectors of maximum and minimum of the generator active powers. $\mathbf{V}_{DC}^{max}$ and $\mathbf{V}_{DC}^{min}$ are the vectors of maximum and minimum DC bus voltages. $\mathbf{P}_{MMC}^{max}$ is the vector of maximum active power that a converter can inject into the AC system. The reactive power of each converter is regulated at zero. Hence, each entry of $\mathbf{P}_{MMC}^{max}$ is equal to the MVA rating of the corresponding MTDC converter. $\mathbf{V}_{AC}^{min}$ and $\mathbf{V}_{AC}^{max}$ represent the minimum and maxi-

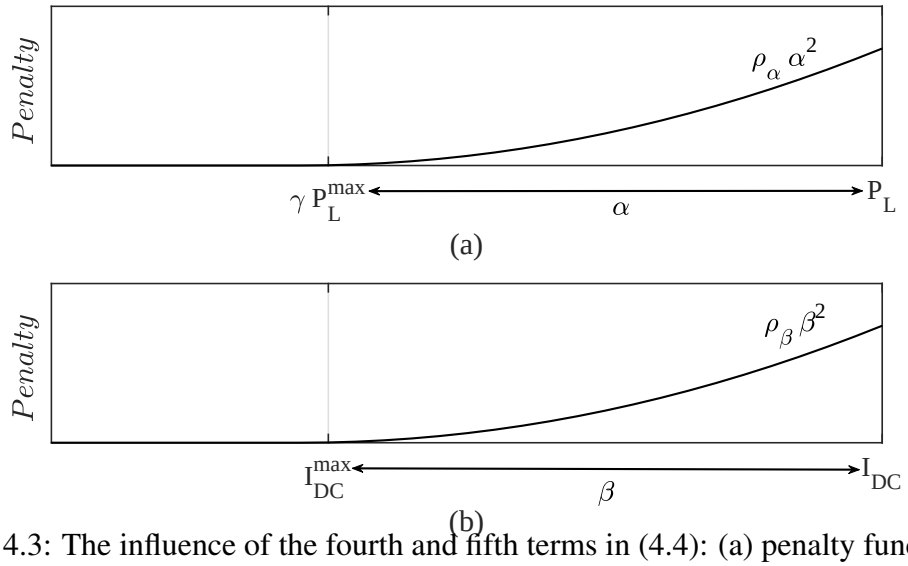

Figure 4.3: The influence of the fourth and fifth terms in (4.4): (a) penalty function corresponding to an AC line constraint, (b) penalty function corresponding to a DC line constraint.

mum AC voltages, respectively. The slack variables in (4.7) and (4.9), smooth the corresponding constraints. As shown in Fig. 4.3(a), the fourth term in (4.4) represents the situation in which the AC line loading reaches its highest level. In this case, the large values of the diagonal entries of ρ_α heavily penalize the controller. The fifth term in (4.4) represents the situation in which the DC current exceeds its limits. As shown in Fig. 4.3(b), its penalty function is similar to the fourth term.

Even though (4.7) helps the controller to alleviate any AC line overloads, defining a proper $\mathbf{P}_L^{target}$ in (4.4) can help the controller to achieve a better performance. The reference values are defined such that the controller proactively alleviates overload of an AC line. In other words, if the loading of an AC line is increasing to reach the limit mentioned by (4.7), the controller tries to alleviate the overload of that AC line. To this end, four levels of AC line loading are considered.

Level 1: Level 1 represents a lightly loaded line and there is no concern over it. The controller prefers to keep the loading of the line at its current level. Therefore, the reference power for this level is defined by

$$P_{L(j)}^{target} = P_{L(j)}^{m}, \text{ if } 0 \leq P_{L(j)}^{m} \leq \gamma_1 P_{L(j)}^{max}, \tag{4.13}$$

where $P_{L(j)}^{m}$ is the absolute value of the last measurement of the j^{th} AC line and γ_1 is a positive constant scalar, which is smaller than one.

Level 2: If loading of a line enters this level, the line is more of a concern for the controller. Hence, the controller prefers to reduce the loading of this line to its minimum value of this level as becomes:

$$P_{L(j)}^{target} = \gamma_1 P_{L(j)}^{max}, \text{ if } \gamma_1 P_{L(j)}^{max} < P_{L(j)}^{m} \leq P_{L(j)}^{max}. \tag{4.14}$$

Level 3: The loading of any line in this level is close to the limits mentioned by (4.7). Hence, the controller should prioritize any line in this level over the lines in Level 2 and Level 1. The

controller could take $P_{L(j)}^{max}$ as the reference to decrease the loading to its minimum value of this level. In this report, $P_{L(j)}^{m} - 2(P_{L(j)}^{m} - P_{L}^{max}(j))$ is intentionally used as the reference. This reference may lie in Level 2, Level 1, or even within a negative range. The main point is that by choosing a smaller value for the reference in this level, the first term of (4.4) becomes larger and consequently, penalizes the controller. The reference value of this level is defined as

$$P_{L(j)}^{target} = P_{L(j)}^{m} - 2(P_{L(j)}^{m} - P_{L}^{max}(j)), \qquad \text{if } P_{L(j)}^{max} < P_{L(j)}^{m} \leq \gamma P_{L(j)}^{max}. \tag{4.15}$$

Level 4: If the loading of a line becomes larger than $\gamma P_{L(j)}^{max}$, the constraint introduced by (4.7) gets violated. Accordingly, not only the reference value introduced by (4.15) is considered for the loading of any AC line in this level, but also the fourth term of (4.4) heavily penalizes the controller [Fig. 4.3(a)].

Since there are not sufficient control inputs to force each AC line power to follow its assigned reference value, the controller prioritizes the lines based on their loading levels. Accordingly, the weighting factors are defined as follow:

$$W_{L(j)} = \begin{cases} w_1, & \text{if } P_{L(j)}^{m} \leq \gamma_1 P_{L(j)}^{max} \\ w_2, & \text{if } \gamma_1 P_{L(j)}^{max} < P_{L(j)}^{m} \leq P_{L(j)}^{max}, \\ w_3, & \text{if } P_{L(j)}^{max} < P_{L(j)}^{m} \end{cases} \tag{4.16}$$

where $0 < w_1 \ll w_2 \ll w_3$.

In addition to the diagonal entries of $\mathbf{W}_L$, tuning the other weighting factors affects the controller response. Selection of the weighting factors generally depends on the system and operator's objective and they are tuned based on the following qualitative criteria:

Tuning ρ_α: When the loading of a line reaches level 4 of its loading, the line is exposed to a severe overload. Hence, ρ_α should be much larger than w_3 to force the controller to reduce the loading of the overloaded AC line.

Tuning ρ_β: Tuning ρ_β determines how much the controller should be penalized if a DC line gets overloaded. A small ρ_β means that the controller allows the DC lines to get overloaded to alleviate the AC line overloads. However, this approach is not safe, as it exposes the MTDC system to the DC line overload issue. Hence, to ensure that the overload alleviation method does not cause any further issue in the MTDC grid, ρ_β is considered to be very large compared to w_3.

Tuning $\mathbf{W}_G$ and $\mathbf{W}_{MMC}$: The relationship between the diagonal entries of $\mathbf{W}_G$ and $\mathbf{W}_{MMC}$ determines the extent to which the MTDC converter stations participate in the AC line overload alleviation method. If the diagonal entries of $\mathbf{W}_{MMC}$ are much larger than the diagonal entries of $\mathbf{W}_G$, the controller can not exploit the MTDC converter stations. On the other side, if the diagonal

entries of $\mathbf{W}_{MMC}$ are very small compared to the diagonal entries of $\mathbf{W}_G$, the controller tries to utilize the MTDC converter stations as much as possible. In this report, the latter option is used to ensure that the controller exploits the MTDC converter station in AC line overload alleviation.

In addition to the inequality constraints mentioned in (4.5)-(4.12), the equality constraints are defined as follow:

$$\mathbf{P}_L(k+i) = \mathbf{P}_L(k+i-1) + \left[\frac{d\mathbf{P}_L}{d\mathbf{P}_G}\right] \Delta\mathbf{P}_G(k+i-1), \tag{4.17}$$

$$\mathbf{P}_{MMC}(k+i) = \mathbf{P}_{MMC}(k+i-1) + \left[\frac{d\mathbf{P}_{MMC}}{d\mathbf{P}^{ref}_{MMC}}\right] \Delta\mathbf{P}^{ref}_{MMC}(k+i-1), \tag{4.18}$$

$$\mathbf{P}_L(k+i) = \mathbf{P}_L(k+i-1) + \left[\frac{d\mathbf{P}_L}{d\mathbf{P}_{MMC}}\right] \left[\frac{d\mathbf{P}_{MMC}}{d\mathbf{P}^{ref}_{MMC}}\right] \Delta\mathbf{P}^{ref}_{MMC}(k+i-1), \tag{4.19}$$

$$\mathbf{V}_{AC}(k+i) = \mathbf{V}_{AC}(k+i-1) + \left[\frac{d\mathbf{V}_{AC}}{d\mathbf{P}_{MMC}}\right] \left[\frac{d\mathbf{P}_{MMC}}{d\mathbf{P}^{ref}_{MMC}}\right] \Delta\mathbf{P}^{ref}_{MMC}(k+i-1), \tag{4.20}$$

$$\mathbf{V}_{AC}(k+i) = \mathbf{V}_{AC}(k+i) + \left[\frac{d\mathbf{V}_{AC}(k+i)}{d\mathbf{P}_G}\right] \Delta\mathbf{P}_G(k+i-1), \tag{4.21}$$

$$\mathbf{I}_{DC}(k+i) = \mathbf{I}_{DC}(k+i-1) + \left[\frac{d\mathbf{I}_{DC}}{d\mathbf{P}^{ref}_{MMC}}\right] \Delta\mathbf{P}^{ref}_{MMC}(k+i-1), \tag{4.22}$$

$$\mathbf{V}_{DC}(k+i) = \mathbf{V}_{DC}(k+i-1) + \left[\frac{d\mathbf{V}_{DC}}{d\mathbf{P}^{ref}_{MMC}}\right] \Delta\mathbf{P}^{ref}_{MMC}(k+i-1), \tag{4.23}$$

$$\sum_{n=1}^{N_{dc}} [P_{MMC\,n}(k+i) - P_{MMC\,n}(k+i-1)] = 0, \tag{4.24}$$

$$\sum_{n=1}^{N_{ac}} [P_{G\,n}(k+i) - P_{G\,n}(k+i-1)] = 0, \tag{4.25}$$

where the sensitivity matrices in (4.18) and (4.23) are derived in [77]. The sensitivity matrix in (4.22) is derived in [78]. Furthermore, the sensitivity matrix $\left[\frac{d\mathbf{P}_L}{d\mathbf{P}_G}\right]$ in (4.17) and $\left[\frac{d\mathbf{P}_L}{d\mathbf{P}_{MMC}}\right]$ in (4.19) are derived based on the DC power flow. The sensivity matrices of the AC voltages with respect to the control inputs, which are introduced by (4.20) and (4.21), are derived from the Jacobian matrix of the AC system, which regularly gets updated, as the new set of measurements is received by the controller. In (4.24), N_{dc} and $P_{MMC\,n}$ are the number of the dispatchable converter stations and the active power of the n^{th} converter station, respectively. Equation (4.24) ensures that sum of the converter active power changes is zero to avoid significant changes of the DC bus voltages. In (4.25), N_{ac} and $P_{G\,n}$ are the number of the AC grid generators and the active power of the n^{th} generator, respectively. Equation (4.25), ensures that sum of the generator active power changes is zero to avoid the AC grid frequency deviation. To ensure that the controller does not compromise the voltage stability of the system, prior to updating the setpoints of the MTDC converter stations

and AC grid generators within each time interval, the modal analysis is checked [79]. To this end, each MTDC converter station is modeled as a load in the AC grid. Then, the Jacobian matrix of the AC grid, i.e., J is computed. Assuming that J is expressed by

$$J = \begin{bmatrix} \mathbf{J}_{P\theta} & \mathbf{J}_{PV} \\ \mathbf{J}_{Q\theta} & \mathbf{J}_{QV} \end{bmatrix}, \tag{4.26}$$

to ensure that subsequent to updating the power sepoints of the MTDC converter stations and AC generators, there will not be any voltage instability in the system, the minimum eigenvalue λ of the reduced Jacobian matrix J_r should be positive. The reduced Jacobian matrix represents the sensitivity of the AC voltage to the reactive power and is derived as

$$\Delta\mathbf{Q} = [\mathbf{J}_{QV} - \mathbf{J}_{Q\theta}\mathbf{J}_{P\theta}^{-1}\mathbf{J}_{PV}]\Delta\mathbf{V}_{AC} = \mathbf{J}_r\Delta\mathbf{V}_{AC}, \tag{4.27}$$

where Q represents the vector of the reactive powers of the AC grid buses.

Although the test system of Fig. 4.4 includes only one AC grid, the proposed method can be generalized to the cases in which different asynchronous AC grids are connected by a MTDC grid. In this case, (4.24) should be considered for each set of the dispatchable converter stations connected to the same AC grid, separately. Similarly, (4.25) should be considered for each AC grid.

4.3 Simulation Results

In this report, the effectiveness of the proposed method on two test systems is investigated. The objective of simulation studies on Test System 1 is to provide detailed discussion on the proposed method, while simulation studies on Test System 2 evaluate the performance and effectiveness of the proposed method on a large AC system. In Test System 1, the AC voltage limits and voltage stability issue are not investigated. All the simulation results are presented in per-unit values. The base DC and AC voltages are equal to 400 kV and 230 kV, respectively. The DC line base current and the based power are equal to 250 A and 100 MW, respectively.

4.3.1 Test System 1

As shown in Fig. 4.4, Test System 1 represents a five-terminal MTDC grid embedded in the New England 39-bus test system. Each generator is equipped with an automatic voltage regulator (AVR), a power system stabilizer (PSS), a governor and a turbine. The detailed information of each component of the AC system can be found in [80]. Furthermore, generators G5, G8, and G9 participate in AGC. The ramp rate of each generator is 0.1 MW/s. Every AC transmission line is modeled using a lumped π-model.

The converter stations of the MTDC system are based on MMC together with all the control loops detailed in [81]. An offshore wind farm is connected through two 250 km cables to buses 2 and 4

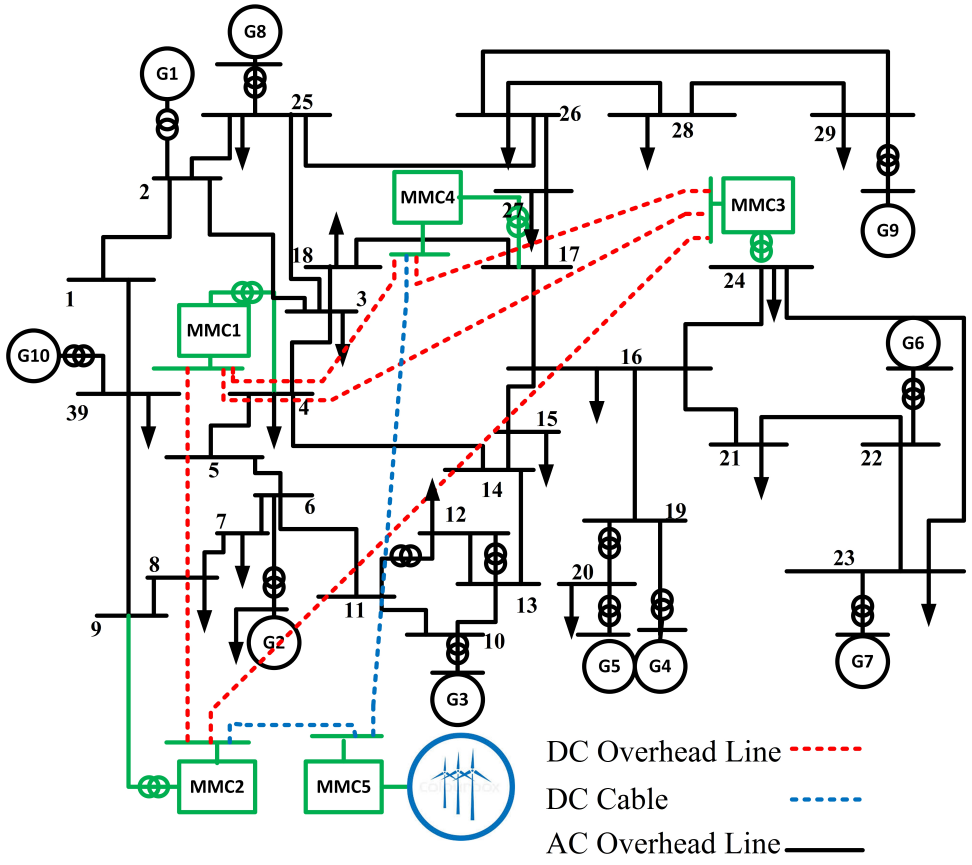

Figure 4.4: The New England 39-bus test system embedded with a 5-bus MTDC system.

of the MTDC system, while the other buses of the MTDC system are connected through overhead DC lines. MMC1, MMC3 and MMC4 operate in $P-V$ droop mode with droop constants of 18, 12, and 20, respectively. MMC2 operates in constant power mode. Moreover, MMC5 absorbs the wind farm power. MMC1 to MMC4 connect the DC buses $1,2,3$, and 4 of the MTDC to AC buses $4,9,24$, and 17, respectively. The maximum and minimum DC bus voltages are 1.09 pu and 0.91 pu, respectively. Conventionaly, the maximum currents of the DC lines and the DC cables are assumed to be equal to their rated currents. However, some HVDC lines have a thermal over current protection to prevent undesired tripping of the line [82]. To avoid this issue, a safety factor is considered and the maximum DC current is assumed to be equal to 90% of the rated current. Consequently, the maximum current of the DC lines and DC cables are 10.8 pu and 7.06 pu, respectively [81]. All the converters except for MMC5 operate in PQ mode at their AC sides. While the converter active powers are determined by the proposed controller, the converter reactive powers are always regulated at zero. The rated powers of MMC1 to MMC5 are 12 pu, 12 pu, 8 pu, 8 pu, and 6 pu, respectively.

In (4.4), all the diagonal entries of $\mathbf{W}_G$ are equal to 1, while the entries of $\mathbf{W}_{MMC}$ are assumed to be 0.001, which means that the controller prioritizes the MTDC converters. The diagonal entries of ρ_α and ρ_β are both equal to 10^5. The required measurements of the controller are received every $t_m = 5$ s. The proposed controller updates the setpoints with a time delay of $t_d = 1$ s due to

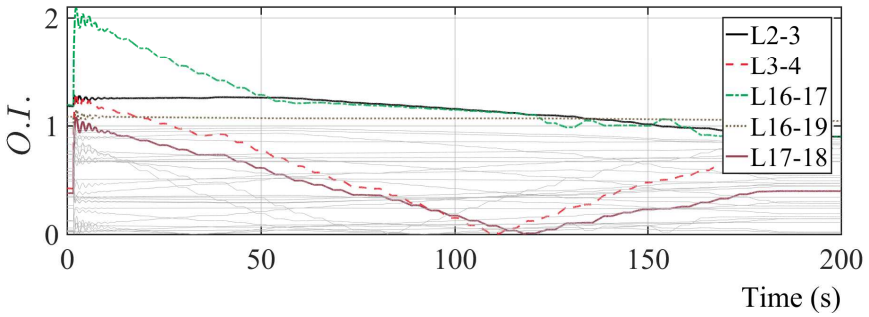

Figure 4.5: System response to the outage of line $L15-16$: O. I.s of the AC lines.

latency in updating setpoints and communication. $T = 200$ s is the determined time for overload alleviation. If the controller fails to relieve all the overloads within 200 s, the operator can reinitiate the controller. The control horizon is assumed to be 3. Regarding (4.16), w_1, w_2, w_3, and γ_1 are assumed to be 1, 10, 1000, and 0.9, respectively. In (4.7), γ is equal to 1.1. For the sake of simplicity in presentation, an *Overload Index* is defined by

$$O.I. = \frac{\textit{active power of the AC line}}{\textit{rated MVA of the AC line}}. \tag{4.28}$$

To create more overloads in the test system, the rated MVA of each AC line in the New England test system is reduced to 80% of its original value.

4.3.2 Scenario a

Assume that at $t = 2$ s, line $L15-16$ gets disconnected. This outage imposes overloads on lines $L2-3$, $L3-4$, $L16-17$, $L16-19$, and $L17-18$. As shown in Fig. 4.5, subsequent to the outage, the controller receives the measurements every 5 s and updates the active power setpoints of the MTDC converter stations and AC generators. Thereby, the AC line overloads slowly get alleviated. Comparison between Fig. 4.6(a) and (b) demonstrates that the MTDC converter stations can play a major role in overload alleviation, as they do not have any ramp rate limit. Regarding Fig. 4.7, as the controller reduces the AC line active powers, it ensures that the DC bus voltages and the DC line currents remain within their acceptable limits. For example, as shown in Fig. 4.7(a), at $t = 57$ s, as the DC bus voltages decrease to the lower bound of the DC bus voltage, the controller smoothly increases the DC bus voltages.

It is worth noting that with respect to Fig. 4.4, since active power of line $L16-19$ is only sensitive to the active powers of generators G4 and G5 , the controller has no choice except for using those generators. This is why the active power of this line varies very slowly.

The active power change of each line from $t = 2$ s to $t = 200$ s is due to both of the AC system generators and the MTDC converters. Figure 4.8 demonstrates that major part of the active power change in most of the AC lines, particularly the overloaded lines, is due to the MTDC converters, because the controller can change the active power setpoint of each MTDC converter much faster

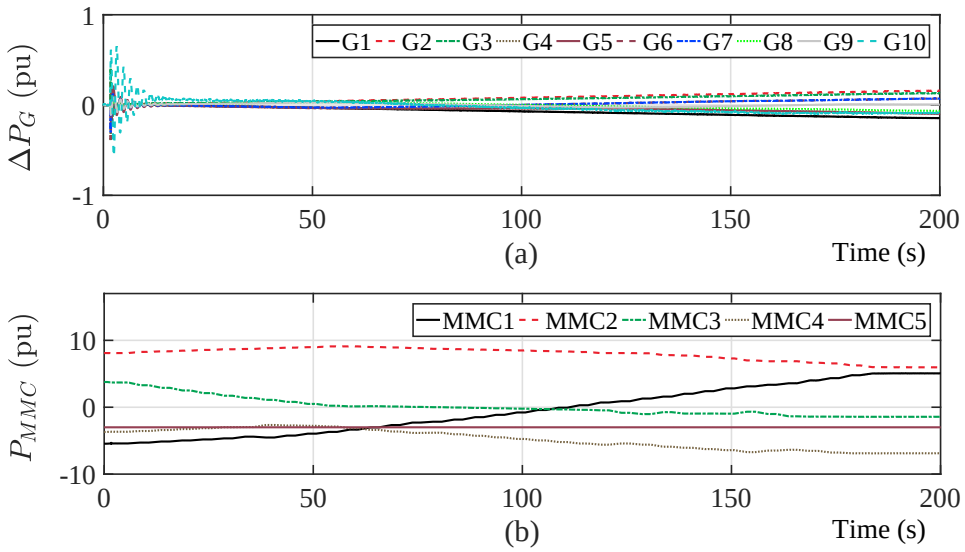

Figure 4.6: System response to the outage of line $L15-16$: (a) AC system generator active powers, and (b) MTDC converter active powers injected into the AC grid.

than the AC system generators. Hence, even the AC line active powers that are less sensitive to the converters' active power setpoints can be substantially influenced by the MTDC converters. There are only a couple of exceptions. With respect to Fig. 4.4, subsequent to the outage of line $L15-16$, line $L14-15$ is the only line that feeds the load at bus 15. Hence, for any intentional active power reduction on this line, the system operator should use load shedding. The other exceptions are lines $L26-28$, $L26-29$, and $L28-29$, which are located near generator $G9$. The last one is line $L16-19$, which was already discussed.

4.3.3 Scenario b

In this scenario, at $t = 2$ s a load at bus 16 with $P = 3.3$ pu and $Q = 0.3$ pu is connected to the AC system.

As shown in Fig. 4.9(a), subsequent to the load energization, lines $L2-3$, $L4-5$, and $L16-19$ become overloaded. Following this contingency, the proposed controller decreases loading of lines $L2-3$ and $L4-5$. Nevertheless, lines $L16-17$ and $L16-24$ temporarily become overloaded. Consequently, the corresponding slack variable factors in vector α in the fourth term of (4.4) are activated, thereby penalizing the controller. Hence, the controller relieves the overloads of lines $L16-17$ and $L16-24$ as fast as possible. Similar to the previous scenario, since the active power of line $L16-19$ is only dependent on the active powers of generators $G4$ and $G5$, its loading varies slowly.

Following the event, the droop mechanism of all the AC system generators and the AGC scheme recover the AC system frequency as shown in Fig. 4.9(b). Variation of the generator active powers from the moment before the load energization to $t = 200$ s for generators G1 to G10 are -0.15 pu,

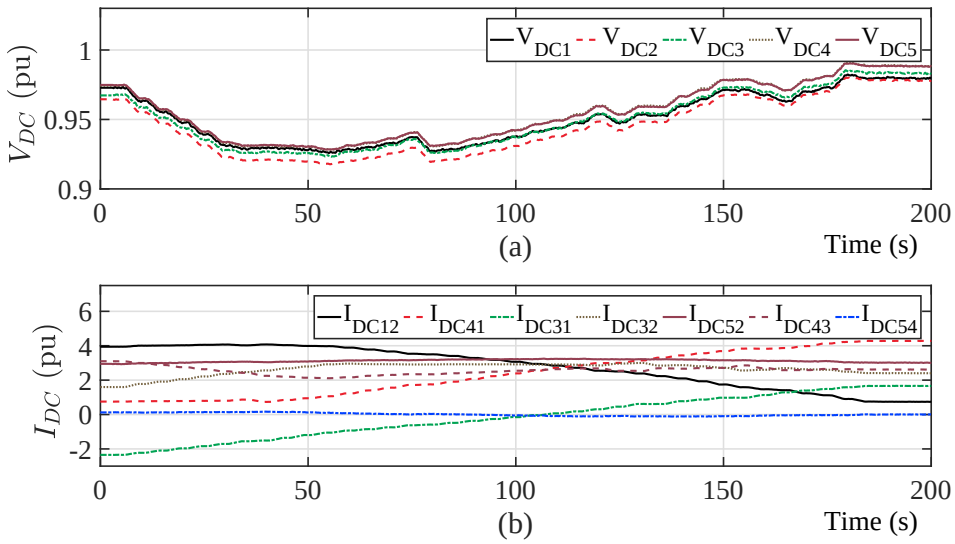

Figure 4.7: System response to the outage of line $L15-16$: (a) DC bus voltages, and (b) DC lines currents.

0.10 pu, 0.6 pu, -0.01 pu, -0.01 pu, 0.15 pu, 0.09 pu, -0.15 pu, 0.43 pu, and 2.15 pu, respectively. Fig. 4.10(a) shows that the active powers of MMC1 to MMC4 change by 10.93 pu, -5.51 pu, -2.25 pu, and -2.88 pu, respectively. The large variations of the generator active powers are due to the AGC and governor actions. Since the proposed controller has no information about the AGC mechanism, all the AGC and the governor actions act like disturbances to the proposed controller. The benefit of using the MTDC converters is that the frequency control scheme has no influence on the MTDC converters. Since the MTDC converters play a major role in overload alleviation of most of the AC lines, the proposed controller manages to alleviate the AC line overloads by substantially changing active power of the MTDC converters. As the control changes the converters' active power setpoints, constraints (4.24) and (4.25) ensure that the proposed strategy does not create any frequency deviation, thereby degrading the frequency control performance. Hence, the proposed method is compatible with the traditional frequency control scheme.

With respect to Figs. 4.10(b) and (c), following the load energization, the controller keeps the DC bus voltages and the DC line currents within their constraints. The DC bus voltage is very close to its lower limit from $t = 75$ s to $t = 125$ s. However, the controller avoid any DC bus voltage violation.

4.3.4 Scenario c

This scenario investigates the influence of a converter outage on the proposed controller. The controller begins to relieve any available overload at $t = 15$ s. As shown in Fig. 4.11, at $t = 27$ s, MMC3 goes out of service. Following the outage, the AC/MTDC system condition entirely changes and some of the AC lines may get overloaded or loading of some of the AC lines may drop. The important event is that the controller losses one of its control inputs. As shown in

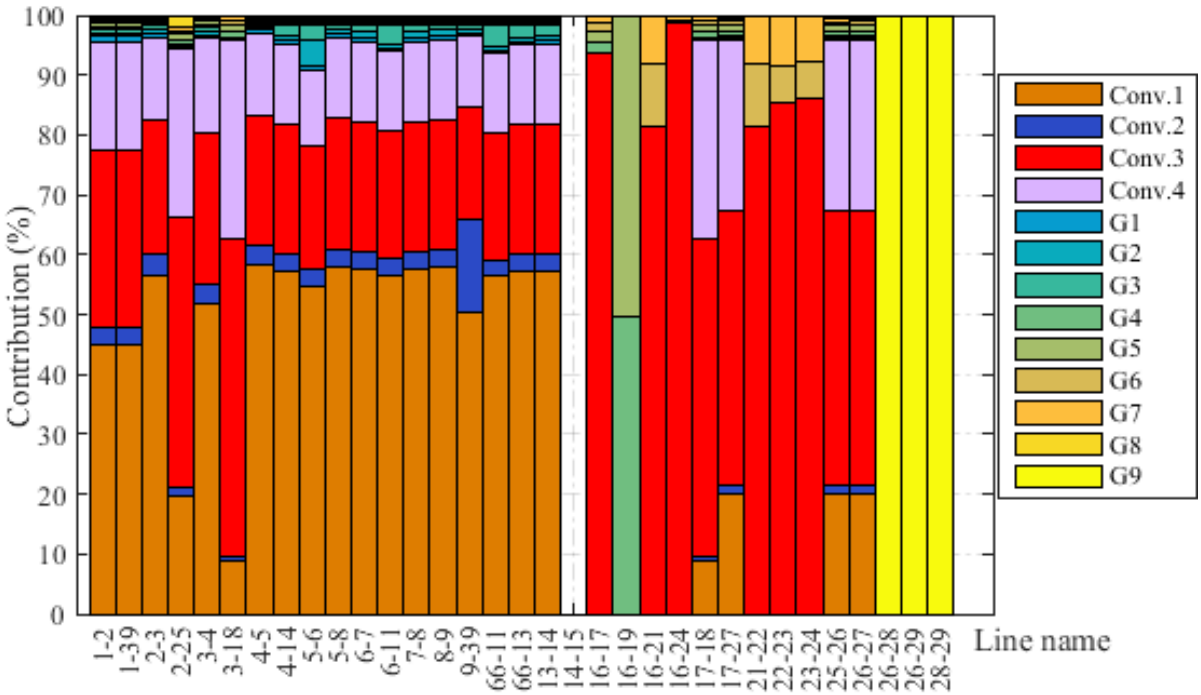

Figure 4.8: System response to the outage of line $L15-16$: share of the MTDC converters and the AC system generators in the AC line active power changes from $t = 0$ s to $t = 200$ s.

Fig. 4.12(a), following the outage, the controller relieves the overload of line $L2-3$ in about one minute but the O. I. of line $L16-19$ decreases from 1.08 to 1.03. As mentioned in the previous scenarios, the active power of this line is only dependent on the active powers of generators G4 and G5. This is why its active power changes very slowly. Another issue which should be taken into consideration is any sudden change of the DC bus voltage. The DC bus voltages experience a considerable jump from 0.97 pu to 1.07 pu, which means that the controller must avoid hitting the upper limit of DC bus voltage while reliving the AC line overloads. Figure. 4.12(b) shows that the voltage remains within its limit over the whole controller implementation period. Furthermore, as shown in Fig. 4.12(c), the controller ensures that the DC line currents do not surpass their thresholds.

4.3.5 Test System 2

As shown in Fig. 4.13, Test System 2 is a 6-bus MTDC grid embedded within the IEEE 118-bus test system. The MTDC grid connects an offshore wind farm at bus 6 to the other onshore converter stations. MMC1 to MMC5 connect the DC buses $1-5$ to the AC buses $17, 47, 51, 79$, and 106, respectively. The rated power of each converter station and the rated current of each DC line are the same as the MTDC grid in Test System 1 unless explicitly mentioned. All the converters except for the MMC6 operate in $P-V$ mode. The rated power of MMC1 and MMC2 is 12 pu while the rated power of MMC3 to MMC6 is 8 pu. The maximum and minimum AC bus voltages are 1.1 pu and 0.9 pu, respectively. Regarding (4.16), w_1, w_2, w_3, w_G, and w_{MMC} are assumed to be 0.01, 1, 10, 1, and 0.1, respectively. In the following scenarios, the controller accommodates

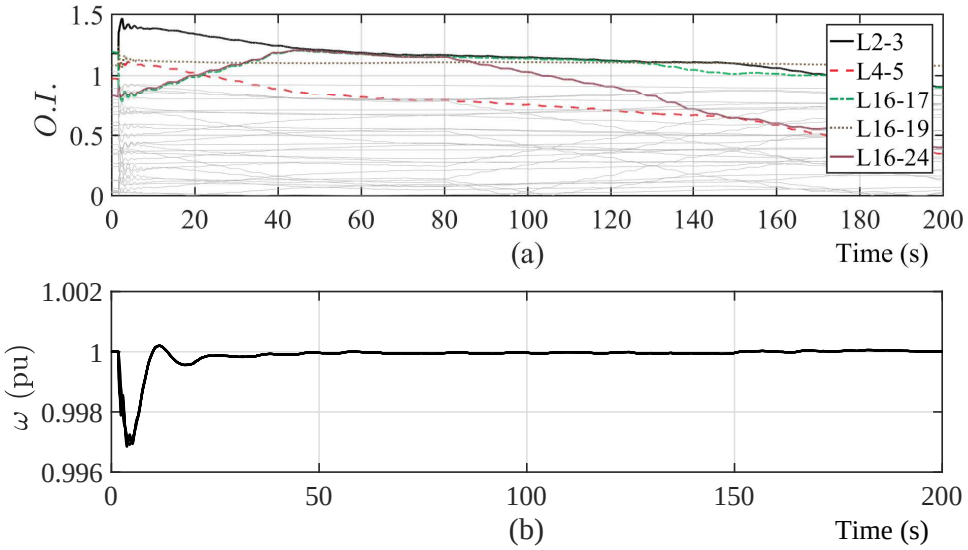

Figure 4.9: System response to energization of a load at bus 16: (a) O. I.s of the AC lines, and (b) frequency of the AC system.

the AC voltage constraints and voltage stability criterion check, which are introduced by (4.8) and (4.27), respectively. All the other control parameters are the same as the parameters of Test System 1.

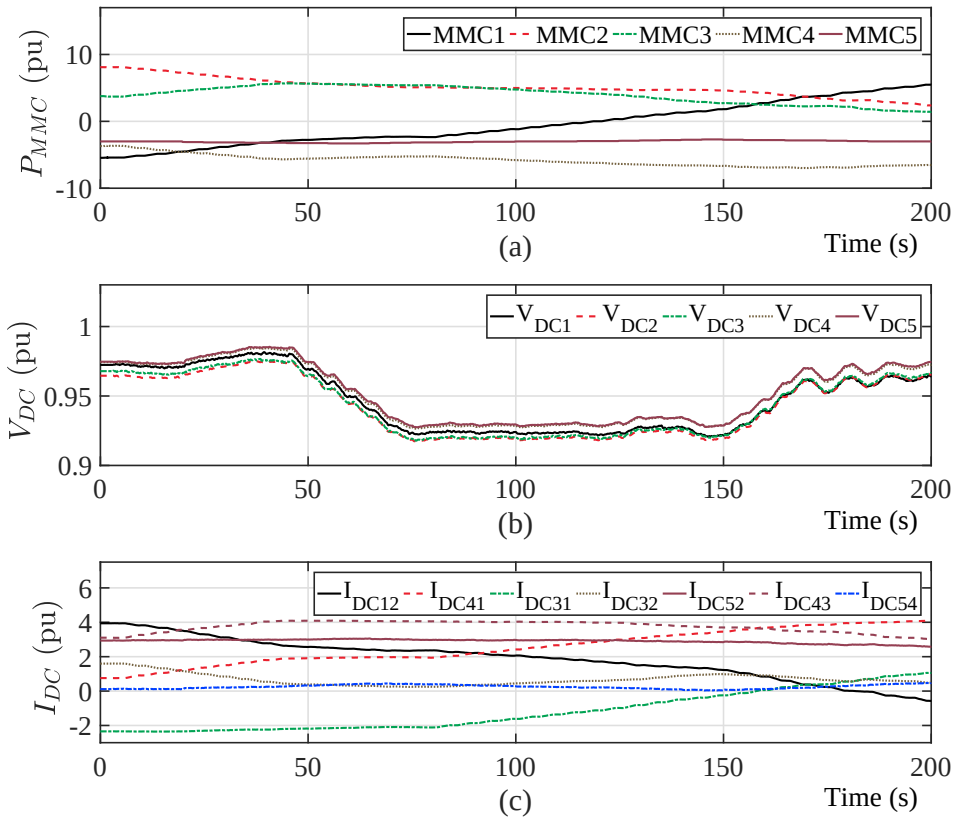

Figure 4.10: System response to energization of a load at bus 16: (a) active powers of the MTDC converters, (b) DC bus voltages, and (c) DC line currents.

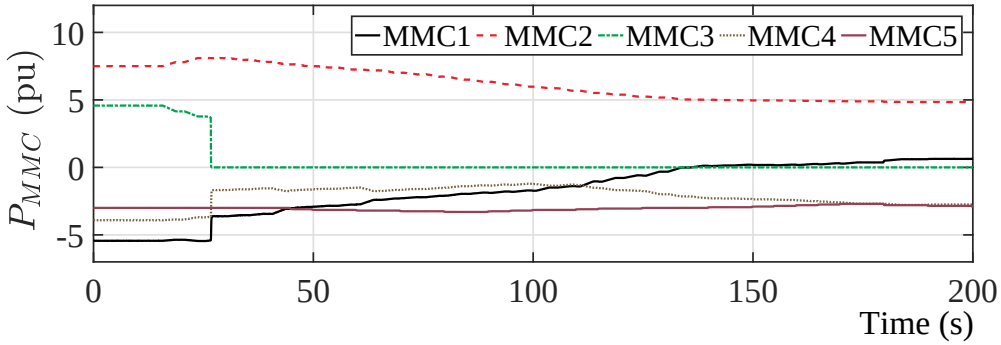

Figure 4.11: Active powers of the MTDC converters following the outage of MMC3.

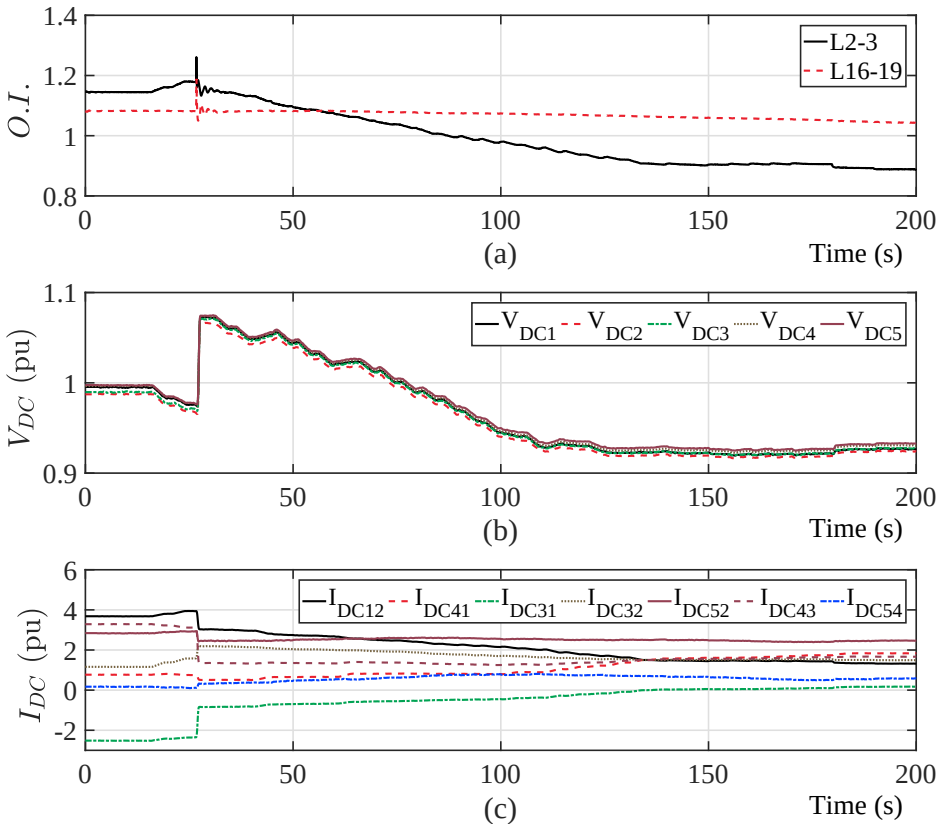

Figure 4.12: System response to the outage of MMC3: (a) O. I.s of lines $L2-3$ and $L16-19$, (b) DC bus voltages, and (c) DC line currents.

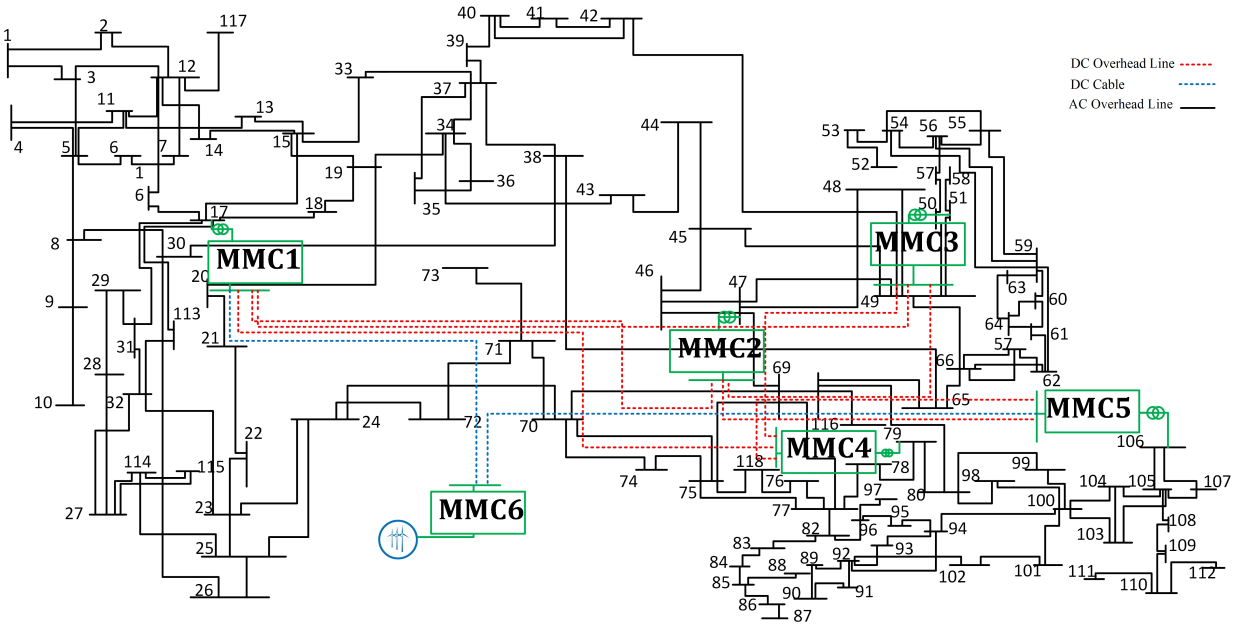

Figure 4.13: A 6-bus MTDC system embedded within the IEEE 118-bus test system.

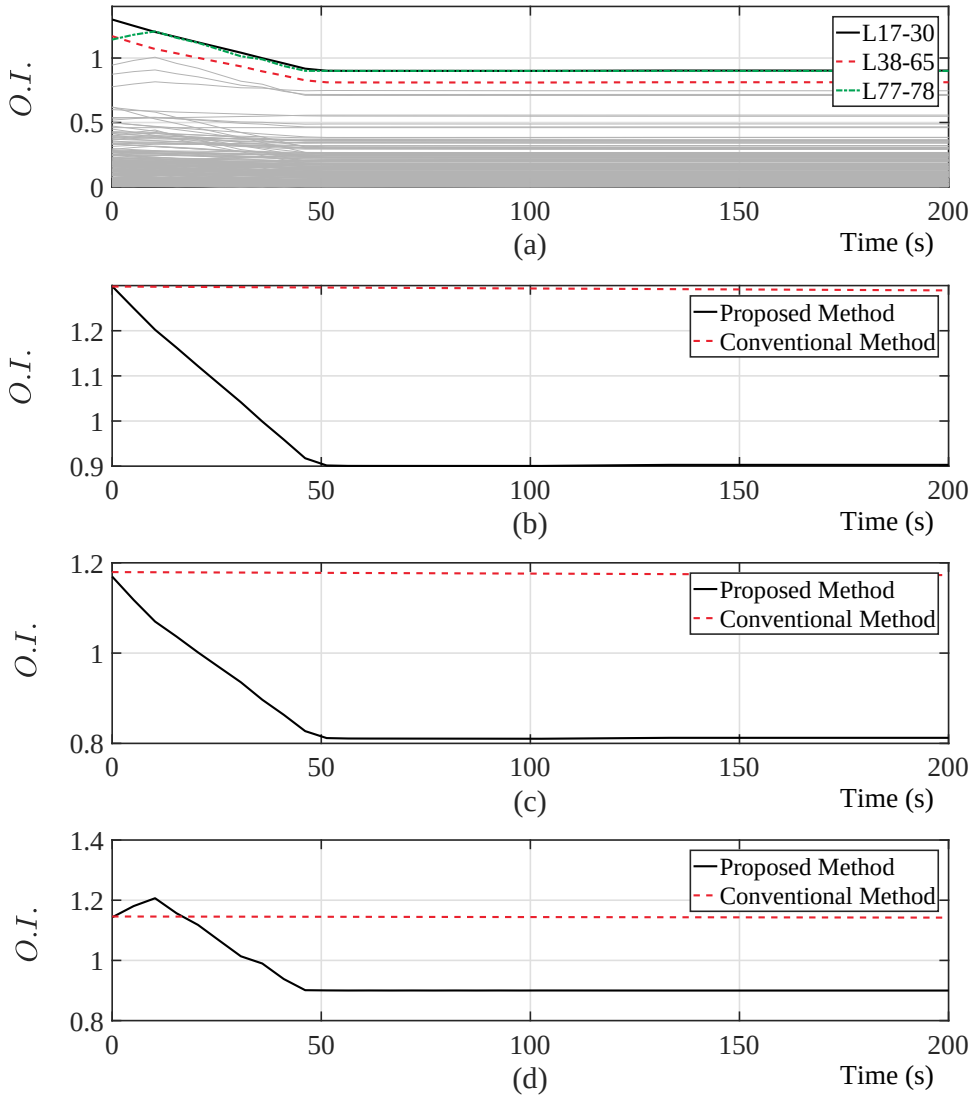

Figure 4.14: Comparison between the proposed and conventional methods: (a) O. I.s of the AC lines, (b) O. I. of line $L17-30$, (c) O. I. of line $L38-65$, and (d) O. I. of line $L77-78$.

4.3.6 Comparison with the conventional method

In this scenario, the proposed method is compared with a conventional method called Linear Programming Optimal Power Flow (LPOPF). The objective function and the constraints of the conventional method are defined as follow:

$$\begin{aligned} &\min_{\Delta P_{G(i)}} \sum_{i=1}^{n} |\Delta P_{G(i)}| \\ &s.t. \sum_{i=1}^{n} \frac{dP_{L(j)}}{dP_{G(i)}} \Delta P_{G(i)} \leq P_{L(j)}^{max} - P_{L(j)}^{m},\ j = 1,2,...,l, \\ &\sum_{i=1}^{n} \Delta P_{G(i)} = 0, \end{aligned} \tag{4.29}$$

where n, l, $\Delta P_{G(i)}$, $P_{L(j)}^{max}$, and $P_{L(j)}^{m}$ represent the number of AC generators, the number of overloaded lines, the power setpoint change of AC generator i, the maximum power of overloaded line j, the power of the overloaded line j at $t = 0$ s. The objective function of (4.29) ensures that power setpoint changes of the AC generators are optimally computed. The inequality constraint ensures that any AC line overload will be alleviated. The equality constraint considers power balance in the system. The optimum power setpoint changes are computed by using linear programming and applied to Test Case 2 by considering the ramp rates of the AC generators. In the conventional method, the MTDC grid does not participate in any overload alleviation.

As shown in Fig. 4.14(a), lines $L17-30$, $L38-65$, and $L77-78$ are experiencing AC line overload. The MTDC grid can play a major role in relieving the lines which are in the vicinity of its AC buses. This is why loading of lines $L17-30$ and $L77-78$ quickly decrease. However, the MTDC grid can reduce the loading of the lines that are located far from its AC buses. Line $L38-65$ is an example, whose loading is sufficiently decreased. Comparison with the conventional method in Figs. 4.14(b)-(d) indicates that the power flow changes of the overloaded lines are very small, as the ramp rate of the AC generators is the major issue in overload alleviation. In this cases, the operator may reluctantly shed some loads to expedite the overload alleviation. Moreover, since (4.29) considers only the overloaded lines, subsequent to overload alleviation, other AC lines may get overloaded. Exploiting the MTDC converter stations not only increases the number of control inputs, but also improves the speed of overload alleviation scheme. The salient advantage of the MPC-based strategy over the conventional method is that it can coordinate the power setpoints of the MTDC converter stations and AC grid generators such that not only the AC line overloads are mitigated but also any new overload does not occur in the system.

4.3.7 Influence of weighting factors

The variation of the weighting factors in the proposed MPC-based strategy, expressed in (4.4), can change the response of the controller. Three cases with different weighting factors, which are introduced in Table 4.1, are compared. Case 1, which is used in other scenarios, is compared with cases 2 and 3 to highlight the impact of weighting factors. As shown in Figs. 4.15(a) and (b), decreasing w_2 and w_3 implies that the controller is less concerned with the lines in levels 2 and

Table 4.1: Three case scenarios with different weighting factors.

	w_1	w_2	w_3	w_{MMC}	w_G
Case 1	0.01	1	10	0.1	1
Case 2	0.01	0.1	1	0.1	1
Case 3	0.01	1	10	10	1

3. It can be inferred that compared to Case 2, Case 1 is a little bit more conservative. Based on (4.4), the second and third terms are considered to help the controller designer to avoid or favor using the MTDC converter stations. Case 3 demonstrates that by increasing the diagonal entries of $\mathbf{W}_{MMC}$, changing the setpoints of the MTDC converter stations leads to larger values of the objective function. Therefore, the controller cannot exploit the MTDC converter stations similar to Case 1. Accordingly, the performance of the controller in Case 1, shown in Fig. 4.15(a), is better than the performance of the controller in Case 3 [Fig. 4.15(c)]. The variations of MTDC converter station setpoints in cases 1 and 3 are shown in Figs. 4.16(a) and (b), respectively. Moreover, the variations of the power setpoints of the AC grid generators in cases 1 and 3 are shown in Figs. 4.16(c) and (d), respectively. With respect to Fig. 4.16(a), since the diagonal entries of W_{MMC} in Case 1 are very small, the controller fully exploits the MTDC grid converter stations. On the other hand, with respect to Fig. 4.16(b), large diagonal entries of W_{MMC} restrict variations of the power setpoints of the MTDC converter stations at about $t = 25$ s. Consequently, comparison of Figs. 4.16(c) and (d) indicates that in Case 3, the controller has to use the AC generators. Hence, the power setpoint changes of the AC generators are nonzero till $t = 135$ s in Fig. 4.16(d).

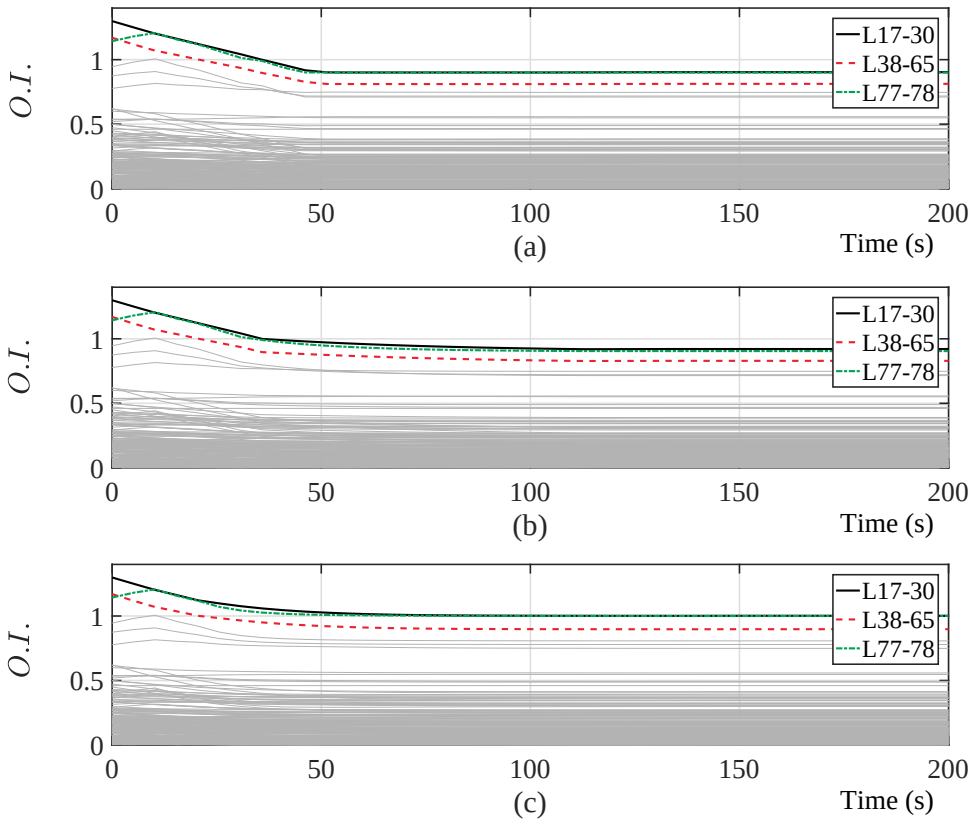

Figure 4.15: Influence of the weighting factors: (a) O. I.s of the AC lines in Case 1, (b) O. I.s of the AC lines in Case 2, and (c) O. I.s of the AC lines in Case 3.

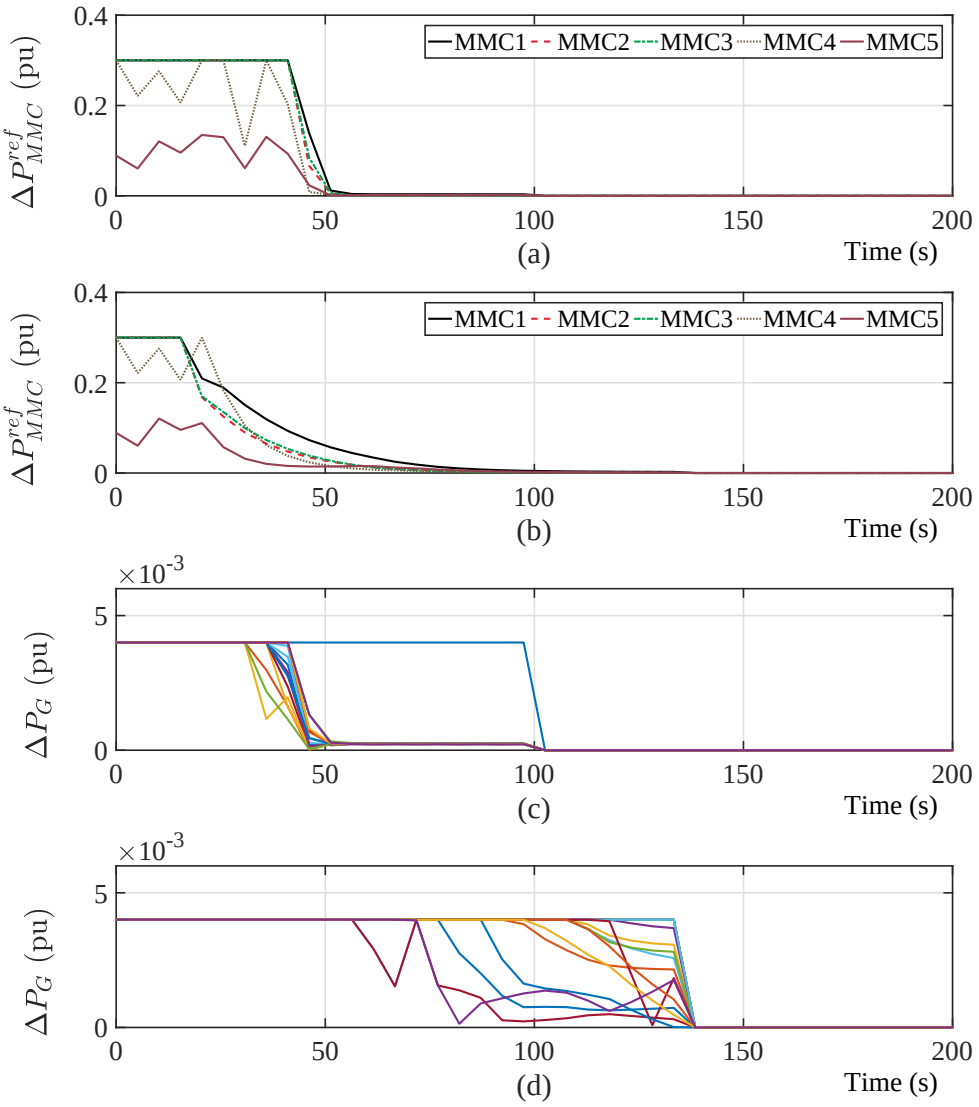

Figure 4.16: Influence of the weighting factors: (a) setpoint changes of the MTDC converter stations in Case 1, (b) setpoint changes of the MTDC converter stations in Case 3, (c) setpoint changes of the AC generators in Case 1, and (d) setpoint changes of the AC generators in Case 3.

4.3.8 Possible limitations of the MTDC grid

There are two important issues which should be taken into consideration: 1) DC line overload, and 2) voltage stability of the AC grid.

DC line overload: If the loading of a DC line reaches its boundaries, the controller should be able to handle both of the AC and DC line overloads. In this scenario, the DC line connecting MMC4 and MMC5 with the rating of 10.8 pu is replaced with another line with the rating of 2.7 pu. Therefore, the controller has to mitigate the overloads of AC and DC lines, simultaneously. Figure 4.17(a) indicates the controller has quickly decreased the loading of the DC line. However, the AC line overload alleviation has a little bit degraded [Fig. 4.17(b)].

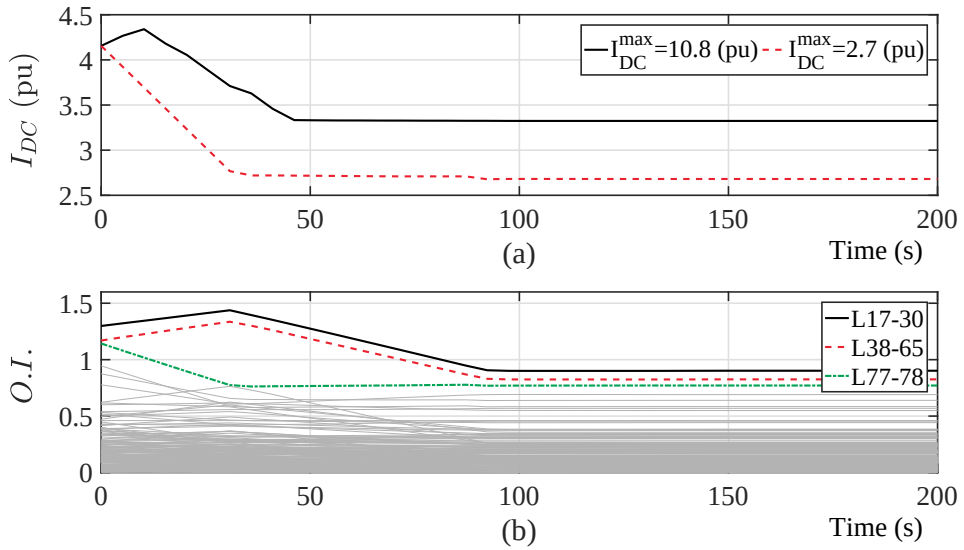

Figure 4.17: Simultaneous DC line and AC line overloads: (a) current of the DC line connecting MMC4 to MMC5, and (b) O. I.s of the AC lines.

Voltage stability: The MTDC grid does not have the ramp rate limits of the AC generators. However, large power variations of the MTDC converter stations may push the system toward the voltage stability boundaries. To avoid this issue, the controller considers the AC voltage constraints and also checks the voltage stability criterion introduced by (4.26) and (4.27) to ensure that the new setpoints do not impose any voltage instability issue on the system. With respect to Fig. 4.18(a), the AC bus voltages always remain within the allowable limits. Furthermore, λ, which denotes the minimum eigenvalue of J_r in (4.27), is always greater than zero and even increases. Accordingly, the system does not experience any voltage instability.

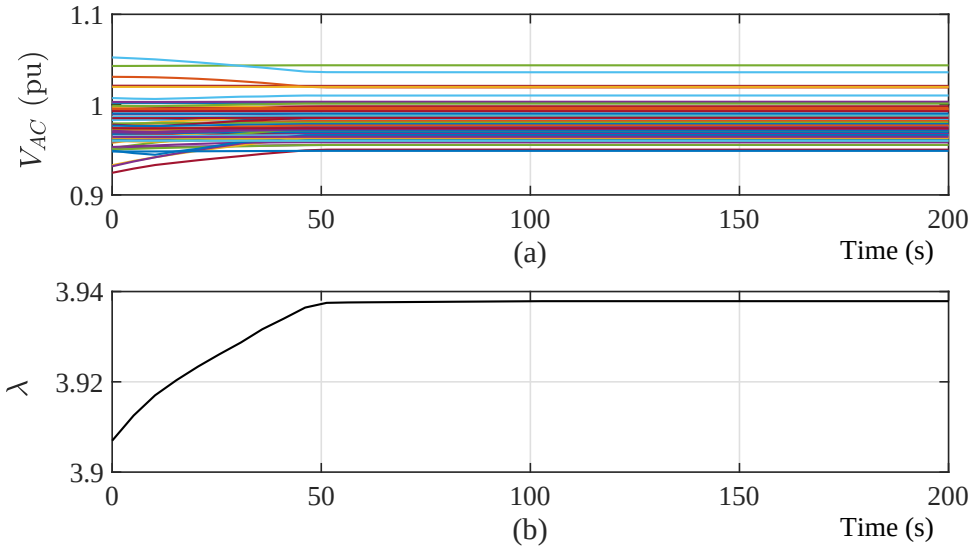

Figure 4.18: AC bus voltage constraint and voltage stability: (a) AC bus voltages, and (b) voltage stability criterion.

4.4 Conclusion

In this report, a model predictive control (MPC)-based overload alleviation scheme for meshed AC/MTDC systems is proposed. The proposed controller is integrated with the conventional AGC and utilizes the MTDC converter stations in conjunction with the AC system generators. The MTDC converter stations play a major role in the proposed controller due to two main reasons: First, the MTDC converter active powers can remarkably change within a short period of time, which expedites the overload alleviation procedure. Secondly, active powers of most of the AC lines are at least a little bit sensitive to the MTDC converters' active power setpoints, which makes the converters effective in active power control of the AC lines. Performance of the proposed controller and the roles of converter stations are evaluated by various case studies on a 5 bus MTDC system integrated with the New England 39-bus test system and a 6 bus MTDC system integrated with the IEEE 118-bus test system.

References

[1] N. Chaudhuri, B. Chaudhuri, R. Majumder, and A. Yazdani, *Multi-terminal Direct-Current Grids: Modeling, Analysis, and Control.* John Wiley & Sons, 2014.

[2] J. Qin, M. Saeedifard, A. Rockhill and R. Zhou, "Hybrid Design of Modular Multilevel Converters for HVDC Systems Based on Various Submodule Circuits," in *IEEE Transactions on Power Delivery*, vol. 30, no. 1, pp. 385-394, Feb. 2015.

[3] J. Cao, W. Du, H. F. Wang and S. Q. Bu, "Minimization of Transmission Lossin Meshed AC/DC Grids With VSC-MTDC Networks," in *IEEE Transactions on Power Systems*, vol. 28, no. 3, pp. 3047-3055, Aug. 2013.

[4] D. Van Hertem and M. Ghandhari, "Multi-terminal VSC HVDC for the European supergrid: Obstacles," *Renewable and Sustainable Energy Reviews*, vol. 14, pp. 3156-3163, 2010.

[5] P.M. Anderson, *Power System Protection*. Hoboken, NJ, USA: J. Wiley & Sons, 1998.

[6] M. Hajian, L. Zhang and D. Jovcic, "DC Transmission Grid With Low-Speed Protection Using Mechanical DC Circuit Breakers," in *IEEE Transactions on Power Delivery*, vol. 30, no. 3, pp. 1383-1391, June 2015.

[7] W. Leterme, S. Pirooz Azad and D. Van Hertem, "Fast breaker failure backup protection for hvdc grids," in *Proceedings of IPST 2015*, Cavtat, Croatia, 2015, pp. 1-6.

[8] W. Leterme, S. Pirooz Azad and D. Van Hertem, "A Local Backup Protection Algorithm for HVDC Grids," in IEEE Transactions on Power Delivery, vol. 31, no. 4, pp. 1767-1775, Aug. 2016.

[9] M. Wang, W. Leterme, J. Beerten and D. Van Hertem, "Robustness evaluation of fast breaker failure backup protection in bipolar HVDC grids," *13th IET International Conference on AC and DC Power Transmission (ACDC 2017)*, Manchester, 2017, pp. 1-7.

[10] V.V Veeravalli and T. Banerjee, *Quickest change detection*. Academic press library in signal processing: Array and statistical signal processing, 2013.

[11] J. Zhao, M. Netto and L. Mili, "A Robust Iterated Extended Kalman Filter for Power System Dynamic State Estimation," in IEEE Transactions on Power Systems, vol. 32, no. 4, pp. 3205-3216, July 2017.

[12] M. Basseville and I. V. Nikiforov, *Detection of abrupt changes: theory and application*. Englewood Cliffs: Prentice Hall, 1993.

[13] T. Routtenberg and Y. Xie, "PMU-base online change-point detection of imbalance in three-phase power systems," 2017 *IEEE Power & Energy Society Innovative Smart Grid Technologies Conference (ISGT)*, Washington, DC, 2017, pp.1-5.

[14] Y. Xie and D. Siegmund, "Sequential multi-sensor change-point detection," *2013 Information Theory and Applications Workshop (ITA)*, San Diego, CA, 2013, pp. 1-20.

[15] W. Leterme, N. Ahmed, J. Beerten, L. Angquist, D. V. Hertem and S. Norrga, "A new HVDC grid test system for HVDC grid dynamics and protection studies in EMT-type software," 11th IET International Conference on AC and DC Power Transmission, Birmingham, 2015, pp. 1-7.

[16] N. Ahmed, L. Angquist, S. Norrga, A. Antonopoulos, L. Harnefors and H. Nee, "A Computationally Efficient Continuous Model for the Modular Multilevel Converter," in

IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 4, pp. 1139-1148, Dec. 2014.

[17] J. Hafner and B. Jacobson, "Proactive Hybrid HVDC Breakers: A key innovation for reliable HVDC grids," in *CIGRE Bologna Symp*., Bologna, Italy, 2011, pp. 1-8.

[18] C.M. Franck, "HVDC Circuit Breakers: A Review Identifying Future Research Needs," in *IEEE Transactions on Power Delivery*, vol. 26, no. 2, pp. 998-1007, April 2011.

[19] M. Pollak, "Optimal detection of a change in distribution," *The Annals of Statistics*, 206-227, 1985.

[20] Tze Leung Lai, "Information bounds and quick detection of parameter changes in stochastic systems," in *IEEE Transactions on Information Theory*, vol. 44, no. 7, pp. 2917-2929, No. 1998.

[21] A. G. Tartakovsky and A. S. Polunchenko, "Quickest changepoint detection in distributed multisensory systems under unknown parameters," *2008 11th International Conference on Information Fusion*, Cologne, 2008, pp. 1-8.

[22] N. Chaudhuri, B. Chaudhuri, R. Majumder, and A. Yazdani, MultiTerminal Direct-Current Grids: Modeling, Analysis, and Control. New York, NY, USA: Wiley, 2014.

[23] D. Van Hertem and M. Ghandhari, "Multi-terminal VSC HVdc for the European Supergrid: Obstacles," Renewable Sustain. Energy Rev., vol. 14, no. 9, pp. 3156-3163, 2010.

[24] C. M. Franck, "Hvdc circuit breakers: A review identifying future research needs," IEEE Trans. Power Del., vol. 26, no. 2, pp. 998-1007, Apr. 2011.

[25] M. K. Bucher and C. M. Franck, "Fault current interruption in multiterminal HVdc networks," IEEE Trans. Power Del., vol. 31, no. 1, pp. 87-95, Feb. 2016.

[26] J. Hafner, "Proactive hybrid HVdc breakers-a key innovation for reliable hvdc grids," in Proc. CIGRE Bologna Symp., 2011, pp. 1-8.

[27] M. Callavik, A. Blomberg, J. Hafner, and B. Jacobson, "The hybrid HVdc Â·· breaker," ABB Grid Syst. Tech. Paper, vol. 361, pp. 143-152, 2012.

[28] J. Sneath and A. D. Rajapakse, "Fault detection and interruption in an earthed HVDC grid using ROCOV and hybrid DC breakers," IEEE Trans. Power Del., vol. 31, no. 3, pp. 973-981, 2016.

[29] L. Graber, S. Smith, D. Soto, I. Nowak, J. Owens, and M. Steurer, "A new class of high speed disconnect switch based on piezoelectric actuators," in Proc. IEEE Electr. Ship Technol. Symp., Jun. 2015, pp. 312-317.

[30] G. C. Lim, T. Damle, and L. Graber, "Optimized contact geometries for high speed disconnect switches," in Proc. IEEE Conf. Electr. Insul. Dielectr. Phenomenon, Oct. 2017, pp. 537-542.

[31] A. Huang, C. Peng, and X. Song, "Design and decelopment of a 7.2kV/200 A hybrid circuit breaker based on 15 kV SiC emitter turnOFF (ETO) thyristor," in Proc. IEEE Electr. Ship Technol. Symp., Jun. 2015, pp. 306-311.

[32] A. Bissal, J. Magnusson, E. Salinas, G. Engdahl, and A. Eriksson, "On the design of ultra-fast electromechanical actuators: A comprehensive multiphysical simulation model," in Proc. 6th Int. Conf. Electromagn. Field Problems Appl., Jun. 2012, pp. 1-4.

[33] P. Skarby and U. Steiger, "An ultra-fast disconnecting switch for a hybrid hvdc breaker-a technical breakthrough," in Proc. CIGRE Canada Conf., 2013, p. 1.

[34] J. Sun, Y. Song, M. Saeedifard, and A. P. Meliopolous, “Sequential tripping of hybrid dc circuit breakers to enhance the fault interruption capability in multi-terminal dc grids,” in Proc. CIGRE US Nat. Committee 2018 Grid of the Future Symp., Oct. 2018, p. 1.

[35] C. Peng et al., “Active damping of ultrafast mechanical switches for hybrid AC and DC circuit breakers,” IEEE Trans. Industry Appl., vol. 53, no. 6, pp. 5354-5364, Nov. 2017.

[36] O. Cwikowski, A. Wood, A. Miller, M. Barnes, and R. Shuttleworth, “Operating DC circuit breakers with MMC,” IEEE Trans. Power Del., vol. 33, no. 1, pp. 260-270, Feb. 2018.

[37] D. Woodgord, “PSCAD user’s guide,” Manitoba HVdc Research Centre, 2003.

[38] P. Magnusson, “Transient wavefronts on lossy transmission lines-effect of source resistance,” IEEE Trans. Circuit Theory, vol. 15, no. 3, pp. 290-292, Sep. 1968.

[39] T. K. Vrana, Y. Yang, D. Jovcic, S. Dennetiere, J. Jardinin, and H. Saad, “The CIGRE B4 dc grid test system,” Electra, vol. 270, no. 1, pp. 10-19, 2013.

[40] R. Wachal et al., “Guide for the development of models for HVdc converters in a HVdc grid,” Tech. Rep., Cigre TB604 (WG B4. 57), Paris, France, 2014.

[41] N. Chaudhuri, B. Chaudhuri, R. Majumder, and A. Yazdani, Multiterminal direct-current grids: Modeling, analysis, and control. John Wiley & Sons, 2014.

[42] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, “Hybrid design of modular multilevel converters for hvdc systems based on various submodule circuits,” IEEE Transactions on Power Delivery, vol. 30, no. 1, pp. 385-394, Feb. 2015.

[43] J. Cao, W. Du, H. F. Wang, and S. Q. Bu, “Minimization of transmission loss in meshed ac/dc grids with vsc-mtdc networks,” IEEE Transactions on Power Systems, vol. 28, no. 3, pp. 3047-3055, Aug. 2013.

[44] M. K. Bucher and C. M. Franck, “Fault current interruption in multiterminal HVDC networks,” IEEE Transactions on Power Delivery, vol. 31, no. 1, pp. 87-95, Feb. 2016.

[45] J. Hafner, “Proactive hybrid HVDC breakers-a key innovation for reliable hvdc grids,” in Proc. CIGRE Bologna Symposium, pp. 1-8, 2011.

[46] C. M. Franck, “Hvdc circuit breakers: A review identifying future research needs,” IEEE Transactions on Power Delivery, vol. 26, no. 2, pp. 998-1007, Apr. 2011.

[47] J. Yang, J. E. Fletcher, and J. O’Reilly, “Multiterminal dc wind farm collection grid internal fault analysis and protection design,” IEEE Transactions on Power Delivery, vol. 25, no. 4, pp. 2308-2318, Oct. 2010.

[48] N. A Belda, C. A. Plet, and R. P. P. Smeets, “Analysis of faults in multiterminal hvdc grid for definition of test requirements of hvdc circuit breakers,” IEEE Transactions on Power Delivery, vol. 33, no. 1, pp. 403-411, Feb. 2018.

[49] M. K. Bucher and C. M. Franck, “Analytic approximation of fault current contributions from capacitive components in hvdc cable networks,” IEEE Transactions on Power Delivery, vo. 30, no. 1, pp. 74-81, Feb. 2015.

[50] W. Mian, J. Beerten, and D. Van Hertem, “Frequency domain based dc fault analysis for bipolar hvdc grids,” Journal of Modern Power Systems and Clean Energy, vol. 5, no. 4, pp. 548-559, 2017.

[51] J. A. Martinez-Velasco and J. Magnusson, “Parametric analysis of the hybrid hvdc circuit breaker,” International Journal of Electrical Power and Energy Systems, vol. 84, pp. 284-295, 2017.

[52] J. A. Corea-Araujo, J. A. Martinez-Velasco, and J. Magnusson, "Optimum design of hybrid hvdc circuit breakers using a parallel genetic algorithm and a matlab-emtp environment," IET Generation, Transmission and Distribution, vol. 11, no. 12, pp. 2974-2982, 2017.

[53] T. K. Vrana, Y. Yang, D. Jovcic, S. Dennetiere, J. Jardini, and H. Saad, "The cigre b4 dc grid test system," Electra, vl. 270, no. 1, pp. 10-19, 2013.

[54] R. Wachal, A. Jindal, S. Dennetiere, H. Saad, O. Rui, S. Cole, M. Barnes, L. Zhang, Z. Song, J. Jardini et al., "Guide for the development of models for hvdc converters in a hvdc grid," Cigre TB604 (WG B4. 57), Paris, Tech. Rep, 2014.

[55] N. Nahman and D. Holt, "Transient analysis of coaxial cables using the skin effect approximation A + Bsqrts," IEEE Transactions on Circuit Theory, vol. 19, no. 5, pp. 443-451, Sep. 1972.

[56] R. L. Wigington and N. S. Nahman, "Transient analysis of coaxial cables considering skin effect," Proceedings of the IRE, vol. 45, no. 2, pp. 166-174, Feb. 1957.

[57] P. Magnusson, "Transient wavefronts on lossy transmission lines-effect of source resistance," IEEE Transactions on Circuit Theory, vol. 15, no. 3, pp. 290-292, Sep. 1968.

[58] J. Lyu, X. Cai, and M. Molinas, "Impedance modeling of modular multilevel converters," in IECON 2015 – 41st Annual Conference of the IEEE Industrial Electronics Society, pp. 180-185, Nov. 2015.

[59] O. Cwikowski, A. Wood, A. Miller, M. Barnes, and R. Shuttleworth, "Operating dc circuit breakers with mmc," IEEE Transactions on Power Delivery, vol. 33, no. 1, pp. 260-270, Feb. 2018.

[60] J. Sneath and A. D. Rajapakse, "Fault detection and interruption in an earthed hvdc grid using rocov and hybrid dc breakers," IEEE Transactions on Power Delivery, vol. 31, no. 3, pp. 973-981, 2016.

[61] J. Sneath, "Grounded hvdc grid line fault protection using rate of change of voltage and hybrid dc breakers," Master's thesis, University of Manitoba, Oct. 2014.

[62] N. Chaudhuri, B. Chaudhuri, R. Majumder, and A. Yazdani, *Multi-terminal Direct-Current Grids: Modeling, Analysis, and Control*: John Wiley & Sons, 2014.

[63] D. Van Hertem, and M. Ghandhari, "Multi-terminal VSC HVDC for the European supergrid: Obstacles," *Renewable and Sustainable Energy Reviews*, vol. 14, no. 9, pp. 3156-3163, 2010.

[64] A. E. Leon, "Short-term frequency regulation and inertia emulation using an MMC-based MTDC system," *IEEE Transactions on Power Systems*, vol. 33, no. 3, pp. 2854-2863, 2018.

[65] N. R. Chaudhuri, R. Majumder, and B. Chaudhuri, "System frequency support through multiterminal DC (MTDC) grids," *IEEE Transactions on Power Systems*, vol. 28, no. 1, pp. 347-356, 2013.

[66] B. Silva, C. L. Moreira, L. Seca, Y. Phulpin, and J. P. Lopes, "Provision of inertial and primary frequency control services using offshore multiterminal HVDC networks," *IEEE Transactions on Sustainable Energy*, vol. 3, no. 44, pp. 800-808, 2012.

[67] L. Harenfors, N. Johansson, L. Zhang, and B. Berggren, "Interarea oscillation damping using active-power modulation of multiterminal HVDC transmissions," *IEEE Transactions on Power Systems*, vol. 29, no. 5, pp. 2529-2538, 2014.

[68] Y. Pipelzadeh, B. Chaudhuri, and Tim C. Green, "Control coordination within a VSC HVDC link for power oscillation damping: A robust decentralized approach using homotopy," *IEEE Transactions on Control Systems Technology*, vol. 21, no. 4, pp. 1270-1279, 2013.

[69] J. Cao, W. Du, and H. F. Wang, "An improved corrective security constrained OPF for meshed AC/DC grids with multi-terminal VSC-HVDC," *IEEE Transactions Power Systems*, vol. 31, no. 1, pp. 485-495, 2016.

[70] K. Meng, W. Zhang, Y. Li, Z. Y. Dong, Z. Xu, K. P. Wong, and Y. Zheng, "Hierarchical SCOPF considering wind energy integration through multi-terminal VSC-HVDC grids," *IEEE Transactions on Power Systems*, vol. 32, no. 6, pp. 4211-4221, 2017.

[71] L. Roald, S. Misra, T. Krause, and G. Andersson, "Corrective control to handle forecast uncertainty: A chance constrained optimal power flow," *IEEE Transactions on Power Systems*, vol. 32, no. 2, pp. 1626-1637, 2017.

[72] J.A. Momoh, J.Z. Zhu, G.D. Boswell, and S. Hoffman, "Power system security enhancement by OPF with phase shifter," *IEEE Transactions on Power Systems*, vol. 16, no. 2, pp. 287-293, 2001.

[73] B. Li, and G. Sansavini, "Effective multi-objective selection of inter-subnetwork power shifts to mitigate cascading failures," *Electric Power Systems Research*, vol. 134. pp. 114-125, 2016.

[74] B. Otomega, A. Marinakis, M. Glavic, and T. Van Custem, "Emergency alleviation of thermal overloads using model predictive control," *Power Tech IEEE Lausanne*, pp. 201-206, 2007.

[75] Almassalkhi, R. Mads, and Ian A. Hiskens., "Model-predictive cascade mitigation in electric power systems with storage and renewables-Part I: Theory and implementation," *IEEE Transactions on Power Systems*, vol. 30, no. 1, pp. 67-77, 2015.

[76] N. Mazzi, B. Zhang, and Daniel S. Kirschen, "An Online Optimization Algorithm for Alleviating Contingencies in Transmission Networks," *IEEE Transactions on Power Systems*, 2018.

[77] T. M. Haileselassie, "Control, Dynamics and operation of multi-terminal VSC-HVDC transmission systems," Ph.D. dissertation, Norwegian Univ. Sci. Technol., 2012.

[78] L. Papangelis, M. S. Debry, P. Panciatici, and T. Van Custem, "Coordinated supervisory control of multi-terminal HVDC grids: a model predictive control approach," *IEEE Transactions on Power Systems*, vol. 32, no. 6, pp. 4673-4683, 2017.

[79] B. Gao, G.K. Morison, and P. Kundur, "Voltage stability evaluation using modal analysis," *IEEE Transactions on Power Systems*, vol. 7, no. 4, pp. 1529-1542, 1992.

[80] C. Canizares, T. Fernandes, E. Geraldi Jr, L. GÃ©rin-Lajoie, M. Gibbard, I. Hiskens, J, Kersulis, R. Kuiava, L. Lima, F. Marco, and N. Martins, "Benchmark systems for small signal stability analysis and control," *https://resourcecenter.ieee-pes.org/pes/product/technical-reports/PESTR18PES-TR*, 2015.

[81] T. K. Vrana, Y. Yang, D. Jovcic, S. DennetiĀre, J. Jardini, and H. Saad, "The CIGRE B4 DC grid test system," *Electra*, vol. 270, no. 1, pp. 10-19, 2013.

[82] Nationa Grid, "Protection and Control for HVDC Systems," *National Grid*, 2014. [online] Available at: https://www.nationalgrid.com.

Part II

A Hybrid Nonlinear Droop Control for MTDC Systems with Improved Dynamic Performance and Stability

Jiangchao Qin
Yuntao Zou

Arizona State University

For information about this project, contact:

Jiangchao Qin
Arizona State University
School of Electrical, Computer, and Energy Engineering
P.O. Box 875706
Tempe, AZ 85287-5706
Fax: 480-727-2052
Email: jqin@asu.edu

Power Systems Engineering Research Center

The Power Systems Engineering Research Center (PSERC) is a multi-university Center conducting research on challenges facing the electric power industry and educating the next generation of power engineers. More information about PSERC can be found at the Center's website: http://www.pserc.org.

For additional information, contact:

Power Systems Engineering Research Center
Arizona State University
527 Engineering Research Center
Tempe, Arizona 85287-5706
Phone: 480-965-1643
Fax: 480-727-2052

Notice Concerning Copyright Material

Table of Contents

1. Introduction 1
2. Principles and Characteristics of the Proposed Hybrid Droop Control 2
    2.1 Principles of the Proposed Hybrid Droop Control 2
    2.2 Characteristic Analysis and Comparison of the Proposed Hybrid Droop Control 3
        2.2.1 Voltage Deviation 4
        2.2.2 Regulation Speed 4
3. Control Structure and Flowchart of the Proposed Hybrid Droop 6
4. Simulation Results 7
    4.1 Performance of the Conventional Linear Droop 7
    4.2 Comparison between the Linear and Proposed Hybrid Droop Control Methods 7
    4.3 Performance of the Proposed Hybrid Droop with Self-Correction Algorithm 9
5. Conclusion 10
References 11

List of Figures

Figure 1. The system diagram of the four-terminal MMC-MTDC System.....2
Figure 2. The operational principles of the conventional linear droop control 3
Figure 3. The operational principles of the proposed hybrid droop control 3
Figure 4. The block diagram of the proposed hybrid droop control.....6
Figure 5. The flowchart of the proposed hybrid droop control.....6
Figure 6. The simulation results of the power reference, measured power, and dc voltage for the conventional linear droop control with k changed from 5 to 40 8
Figure 7. The simulation results of the power reference, measured power, and dc voltage for (1) the proposed droop (k = 20, α = 8), (2) the linear droop control with the steep slop (k = 20, α = 0), and (3) the linear droop control with the shallow slop (k = 50, α = 0). 8
Figure 8. The simulation results of the power reference, measured power, and dc voltage for the proposed droop control (1) with reference self-correction and k = 20, α = 8, (2) without reference self-correction and k = 20, α = 8. 9

List of Tables

Table 1. Electrical Parameters of Simulation Model 7

1. Introduction

Droop control is extensively applied to MTDC systems. VSC-based MTDC systems employ dc voltage to assign imbalanced active power based on droop principle [1] [2]. Fast dynamic response and low voltage fluctuation are expected for bulk dc power transmission. The dc voltage regulation speed and deviation of droop control depends on the first-order derivative and variation of its droop curve. However, in the case of large active power disturbance, the constant derivative of the linear droop curve leads to large voltage deviation and longtime regulation. On the other side, the shallow slop makes the injected power being very sensitive to the dc voltage, which tends to arouse large power oscillation, even though it has better performance on regulation speed and voltage deviation during a transient. Recently, to further improve the performance of droop control, some improved methodologies have been proposed based on self-adjusting slope and nonlinear droop curve [3]–[6]. Reference [3] proposes a self-adjusting slope of droop curve by calculating load fluctuation. However, this method locates the terminals of droop line under extreme operating conditions and the slopes will be adjusted only when they change. Reference [4] gives a variable droop coefficient which is obtained based on the derivative and variation sign of the dc voltage. Although this method can improve regulation speed and reduce voltage deviation, the proposed formula may calculate the positive feedback slope which will cause instability. Reference [5] provides a nonlinear droop regulation to achieve optimal power flow for the purpose of minimizing power losses. But its droop curve consists of piecewise linear segments derived from several offline optimized power flow solutions. Reference [6] proposes a nonlinear droop control based on a polynomial expression to improve power sharing and voltage regulation. However, the derivative of the proposed droop curve depends on the operating point and cannot ensure the constant performance on regulation speed and voltage deviation under different disturbances.

In this report, a new hybrid droop control is proposed to improve the dynamic performance of the VSC-MTDC systems. The features of proposed method are shown as follows:

- Due to the cubic accelerated term, the proposed method provides faster regulation speed and lower voltage deviation than that of the conventional linear one.
- A reference self-correction algorithm is developed to adjust the coefficients of droop curve after recovery. Voltage deviation from droop law is eliminated by this way in steady state. Therefore, the cubic term can be neglected and the proposed droop curve acts as a linear one with small voltage sensitivity and strong stability.
- The proposed method utilizes reference self-correction algorithm to prevent negative influence on derivative by operating point. Thus, the performance of regulation speed and voltage deviation is only affected by imbalanced power and not changed with different operating points.

To verify the effectiveness of the proposed method, the performance of a four-terminal MMC-based HVDC system is investigated based on the proposed method in the PSCAD/EMTDC software environment.

2. Principles and Characteristics of the Proposed Hybrid Droop Control

2.1 Principles of the Proposed Hybrid Droop Control

In this report, a four-terminal ±500 kV three-pole HVDC system is employed as the study system shown in Fig. 1. Assuming that *i*th station uses the droop control, the conventional linear and proposed hybrid droop methods are described in (1) and (2), respectively. All coefficients of these two equations are positive.

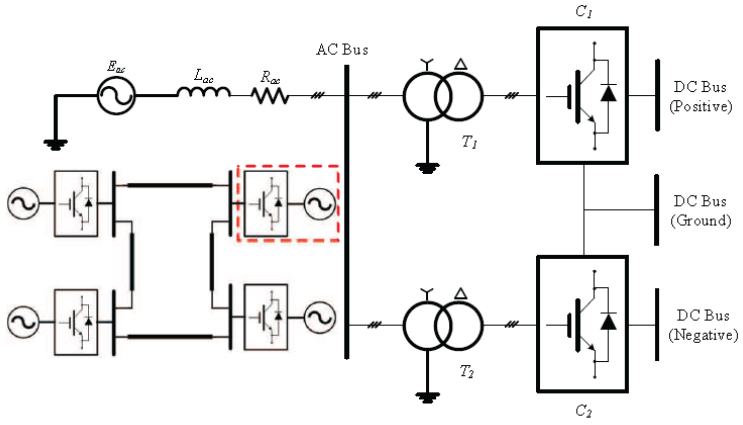

Fig. 1 The system diagram of the four-terminal MMC-MTDC System.

$$P_i = -k\left(U_i - U_{ref}\right) + P_{ref} = -k\Delta U_i + P_{ref} \tag{1}$$

$$P_i = -\alpha\left(U_i - U_{ref}\right)^3 - k\left(U_i - U_{ref}\right) + P_{ref} = -\alpha\Delta U_i^3 - k\Delta U_i + P_{ref} \tag{2}$$

The nonlinear term in (2) must be odd-order exponential to ensure that the derivative of droop curve is positive semi-definite to achieve negative feedback. To prevent over-speed regulation, the cubic term is selected. The coefficients of the proposed hybrid droop U_{ref} and P_{ref} can be adjusted online through the developed reference self-correction algorithm.

Figures 2 and 3 show the operational principles of the conventional linear and proposed hybrid droop control, respectively. For the conventional droop control of Fig. 2, in the case of power change or interruption, the operating point with dc voltage U_i and active power reference P_{ref}, will move along the droop line to a new steady-state point with U_i' and P_{ref}'. However, the linear line of Fig. 2 with the steep slope has small voltage ripple under steady state conditions but it has longtime regulation and large voltage deviation. While, the linear line with the shallow slope has better performance on regulation speed and voltage deviation but it causes power oscillation due to its excessive sensitivity to the dc voltage ripple.

For the proposed hybrid droop control, In the steady state, (2) can be approximated to a linear droop (1) by ignoring minor value of the cubic acceleration term. During a large disturbance, the cubic term can accelerate voltage regulation. On the other hand, the developed reference self-correction moves the droop curve to the new operating point, as shown in Fig. 3. The original operation point A moves to point B by following the red small arrows along the nonlinear curve after performing the reference self-correction algorithm. Therefore, in this way, the proposed

method can ensure the same regulation speed and voltage deviation for different operating points, compensating the defect of the conventional nonlinear droop control.

$$\left|\sqrt[3]{\alpha}\Delta U_i\right|<1\Rightarrow\Delta U_i\in\left(-\frac{1}{\sqrt[3]{\alpha}},\frac{1}{\sqrt[3]{\alpha}}\right) \tag{3}$$

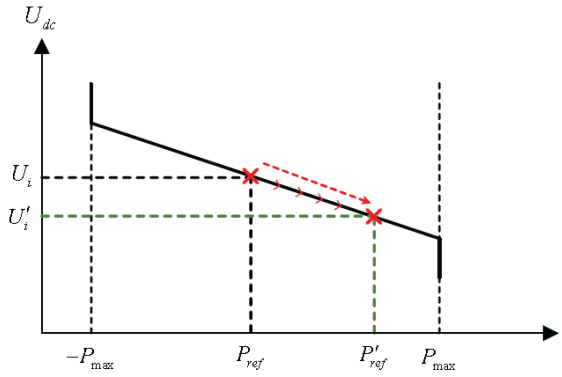

Fig. 2 The operational principles of the conventional linear droop control.

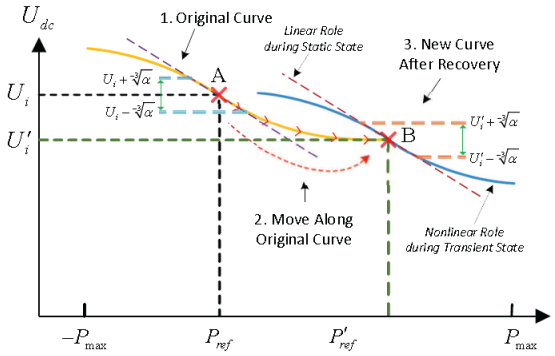

Fig. 3 The operational principles of the proposed hybrid droop control.

The coefficient α in (2) is determined by (3) so that the small value of the cubic term can be neglected during steady state. So in Fig. 3, the approximated linear curves in the intervals of $(U_i-\sqrt[-3]{\alpha},U_i+\sqrt[-3]{\alpha})$ and $(U_i'-\sqrt[-3]{\alpha},U_i'+\sqrt[-3]{\alpha})$ are obtained, respectively, as shown in Fig. 3.

2.2 Characteristic Analysis and Comparison of the Proposed Hybrid Droop Control

In this section, the conventional linear and proposed hybrid droop curves are compared in regulation speed and voltage deviation. Two assumptions are made for the analysis:

- Power loss of the overhead transmission lines and the stored energy in line inductance are considered as constant since the dc current variation is small.
- The dynamics of the converter controller is neglected and the injected power tracks its command instantaneously.

Simple π-section circuit is applied to modeling the overhead transmission lines. Thus, the stored energy in the equivalent capacitors supports the dc voltage and can be calculated by

$$E_{dc}=\sum_{i=1,i\neq j,k}^{4}\frac{1}{2}\left(C_{ij}+C_{ik}\right)U_i^2=\sum_{i=1}^{4}\frac{1}{2}\bar{C}_iU_i^2\ , \tag{4}$$

where C_{ij} and C_{ik} are the equivalent capacitances of the transmission lines of *i*-to-*j* and *i*-to-*k*. Assuming E_{dc0} is the initial stored energy, the energy variation is the integration of the active power of each terminal and described as (5).

$$\sum_{i=1}^{4}\frac{1}{2}\bar{C}_iU_i^2-E_{dc_0}=\int_{0_+}^{t}\left[\sum_{i=1}^{4}P_i-P_{loss}\right]dt=\int_{0_+}^{t}\Delta\bar{P}dt \tag{5}$$

where $\Delta\bar{P}$ is algebraic summation of active power of each terminal and P_{loss} is the equivalent power loss. Generally, the integrand is zero under steady state conditions. During a transient, substituting the small-signal equation $U_i = U_{i0} + \Delta U_i$ into (5) and rearranging it as

$$\sum_{i=1}^{4} \frac{1}{2} C_i \left(2U_{i0}\Delta U_i + \Delta U_i^2 \right) = \int_{0_+}^{t} \Delta\bar{P} dt \tag{6}$$

Assuming that station #1 employs the droop control, and defining that α_i and β_i are per-unit coefficients of the steady state voltage U_{i0} and small signal ΔU_i with the base value U_{10} and ΔU_1, U_{i0} and ΔU_i can be expressed as

$$U_{i0} = \alpha_i U_{10}, \quad \Delta U_i = \beta_i \Delta U_1 \tag{7}$$

The coefficients locate at a small neighborhood of one with small variations.

Substituting (7) into (6), we obtain

$$\int_{0_+}^{t} \Delta\bar{P} dt = U_{10}\Delta U_1 \sum_{i=1}^{4} C_i \alpha_i \beta_i + \Delta U_1^2 \sum_{i=1}^{4} C_i \beta_i^2 = U_{10}\Delta U_1 \gamma_i + \Delta U_1^2 \phi_i \tag{8}$$

where γ_i and ϕ_i are equivalent proportional coefficients and the values of them are evidently positive and in the neighborhood of one. Using $P_1 = P_{ref} - f(\Delta U_1)$ as a generalized form for droop control and substituting it into (8), we obtain

$$\int_{0_+}^{t} \Delta\bar{P} dt = \int_{0_+}^{t} \left[\sum_{i=2}^{4} P_i + P_{ref} - f\left(\Delta U_1\right) - P_{loss} \right] dt = \int_{0_+}^{t} \left[P_\delta - f\left(\Delta U_1\right) \right] dt \tag{9}$$

where $P_\delta = \sum_{i=2}^{4} P_i + P_{ref} - P_{loss}$. Taking the derivative of (8) and (9) in terms of time, then we obtain

$$\gamma_i U_{10} \frac{d\Delta U_1}{dt} + 2\phi_i \Delta U_1 \frac{d\Delta U_1}{dt} = P_\delta - f\left(\Delta U_1\right) \tag{10}$$

Based on (1), (2), and (10), the performance of the droop control can be evaluated on regulation speed and voltage deviation.

2.2.1 Voltage Deviation

To calculate the voltage deviation in steady state after regulation by droop control, the derivative terms in (10) should be zero and, consequently, $P_\delta = f(\Delta U_1)$. According to (1) and (2), $f(\Delta U_1) = k\Delta U_1$ for the conventional linear droop and $f(\Delta U_1) = \alpha\Delta U_1^3 + k\Delta U_1$ for the proposed hybrid droop. Therefore, the power difference P_δ can be expressed for the conventional linear and proposed hybrid droop, respectively, shown as follows:

$$P_\delta = k\Delta U_{1_{CD}} \tag{11}$$

$$P_\delta = \alpha\Delta U_{1_{HD}}^3 + k\Delta U_{1_{HD}} \tag{12}$$

where CD and HD represent the conventional linear droop and proposed hybrid droop, respectively. According to (11) and (12), for same P_δ and identical initial operating conditions, ΔU_{1HD} will be obviously less than ΔU_{1CD}. Therefore, the voltage deviation of the hybrid droop is small than that of the conventional linear droop under steady-state conditions.

2.2.2 Regulation Speed

To compare the regulation speed between the conventional and hybrid droop control methods, Lagrange's mean value theorem is employed. Based on (10), the second-order derivative of ΔU_1 can be expressed by

$$\frac{d^2\Delta U_1}{dt^2}(t)=\frac{d\left(\frac{d\Delta U_1}{dt}\right)}{dt}=\frac{d\left(\frac{d\Delta U_1}{dt}\right)}{d\Delta U_1}\frac{d\Delta U_1}{dt}=\frac{-\left[\gamma_i U_{10}+\phi_i\Delta U_1\right]f'(\Delta U_1)-\phi_i\left[P_\delta-f(\Delta U_1)\right]}{\left(\gamma_i U_{10}+2\phi_i\Delta U_1\right)^3} \quad (13)$$

Substituting $f(\Delta U_1)=k\Delta U_1$ and $f(\Delta U_1)=\alpha\Delta U_1^3+k\Delta U_1$ into (13) for the conventional and proposed droop methods, respectively, and we obtain

$$\left.\frac{d^2\Delta U_1}{dt^2}\right|_{CD}(t)=-\frac{\gamma_i U_{10}k+\phi_i P_\delta}{\left(\gamma_i U_{10}+2\phi_i\Delta U_1\right)^3} \quad (14)$$

$$\left.\frac{d^2\Delta U_1}{dt^2}\right|_{HD}(t)=-\frac{\gamma_i U_{10}k+\phi_i P_\delta}{\left(\gamma_i U_{10}+2\phi_i\Delta U_1\right)^3}-\frac{\Delta U_1^2\alpha\left(3\gamma_i U_{10}+2\phi_i\Delta U_1\right)}{\left(\gamma_i U_{10}+2\phi_i\Delta U_1\right)^3} \quad (15)$$

The numerator of the second term of (15) is always positive since U_{10} is much greater than ΔU_1. Thus, (15) is always greater than (14). Based on Lagrange's mean value theorem, (16) and (17) can be derived and expressed as

$$\left.\frac{d\Delta U_1}{dt}\right|_{CD}(t_{CD})-\left.\frac{d\Delta U_1}{dt}\right|_{CD}(0)=0-\frac{P_\delta}{\gamma_i U_{10}}=t_{CD}\cdot\frac{d^2\Delta U_1}{dt^2}(\zeta_{CD}) \quad (16)$$

$$\left.\frac{d\Delta U_1}{dt}\right|_{HD}(t_{HD})-\left.\frac{d\Delta U_1}{dt}\right|_{HD}(0)=0-\frac{P_\delta}{\gamma_i U_{10}}=t_{HD}\cdot\frac{d^2\Delta U_1}{dt^2}(\zeta_{HD}) \quad (17)$$

The second terms at the left-hand side of (16) and (17) are equal under the same initial conditions. The first terms at the left-hand side of (16) and (17) are zero since the system reaches the new steady-state operating points at t_{CD} and t_{HD}, respectively. By comparing (16) and (17), the time instant t_{HD} is less than t_{CD} since the second-order derivative of the proposed hybrid droop is greater than that of the conventional linear droop. Therefore, the proposed hybrid droop has faster regulation speed than the conventional linear droop.

3. Control Structure and Flowchart of the Proposed Hybrid Droop

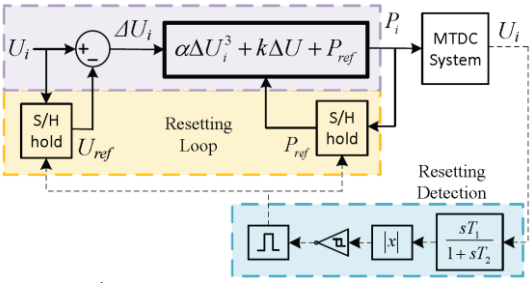

Fig. 5 The flowchart of the proposed hybrid droop control.

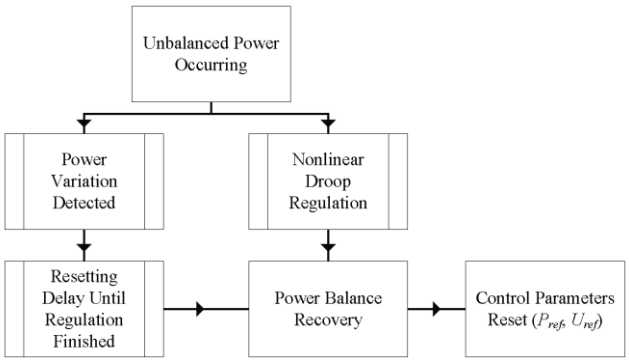

Fig. 4 The block diagram of the proposed hybrid droop control.

The overall structure of the proposed hybrid droop control method is shown in Fig.4. The resetting detection block is used to determine the time instant to perform the reference self-correction algorithm. The resetting loop is triggered by the resetting detection block and used to correct the reference value. After regulation and system recovery, the present voltage U_i and P_i are sampled for the reference U_{ref} and P_{ref} resetting though sample/hold component. Thus, ΔU_i is eliminated and hybrid droop curve moves to the new operation point shown as Fig. 3. The overall procedure as a flowchart is shown in Fig. 5.

4. Simulation Results

4.1 Performance of the Conventional Linear Droop

The parameters of the study system of Fig. 1 are shown in Table I. The parameters of the overhead transmission lines are obtained based on [7].

The performance of the conventional linear droop control with a shallow slope is investigated and the simulation results are shown in Fig. 6. For the shallow slop of Fig. 2, the coefficient *k* in (1) has a large value and, consequently, the output power reference of the droop controller is very sensitive to the dc voltage ripple. As shown in Fig. 6, the ripple of the output power reference from the droop controller increases and this phenomenon will affect the measured active power. Moreover, it increases the dc voltage ripple. Therefore, the shallow slope of the conventional linear droop control causes large ripple as compared with the steep slope under steady state conditions.

Table 1 Electrical Parameters of Simulation Model

Component	Parameters	Symbol	Value	Units
AC Grid	L-L Voltage	U_{ac}	550	kV
	Resistance	R_{ac}	34.895	Ω
	Frequency	f_{ac}	50	Hz
Trans-former	Capacity	S_t	1700	MVA
	Positive Sequence Leakage Reactannce	X_t	0.15	$p.u.$
	Primary Winding Voltage (YN)	U_{1t}	525	kV
	Secondary Winding Voltage (Δ)	U_{2t}	260	kV
MMC	Capacity	S_{MMC}	1500	MVA
	Capacitor of SM	C_{SM}	15	mF
	Voltage of SM	V_{SM}	2.293	kV
	Amount of SM	n_{SM}	218	
	Inductor of Arm	L_0	0.1	H
	Equivalent Resistance of Arm	R_0	3.5	Ω
	Resistance of Connected Lines	R_L	1	Ω
	Inductor of Filter	L	0.05	H

4.2 Comparison between the Linear and Proposed Hybrid Droop Control Methods

The simulation results of the proposed hybrid droop control (k = 20, α = 8) and the conventional linear droop control with the steep and shallow slopes are shown in Fig. 7. As shown in Fig. 7, the conventional linear droop control with the shallow slope (k = 50, α = 0) has the faster regulation speed and less voltage deviation than that of the linear droop with the steep slope (k = 20, α = 0) during a transient. However, the linear droop curve with the shallow slope has larger ripples in the power reference, measured power, and dc voltage under steady state conditions. On the other hand, the regulation speed of the proposed droop is similar to that of the linear droop with the shallow slop. However, the voltage deviation of the proposed droop is smaller than both linear droop curves with steep and shallow slope. The ripples of the proposed hybrid droop in the power reference, measured power, and dc voltage under steady state conditions are less than both ones as well.

Therefore, the proposed hybrid droop with the developed reference self-correction algorithm achieves the better performance than the conventional linear droop under both dynamic and steady state conditions.

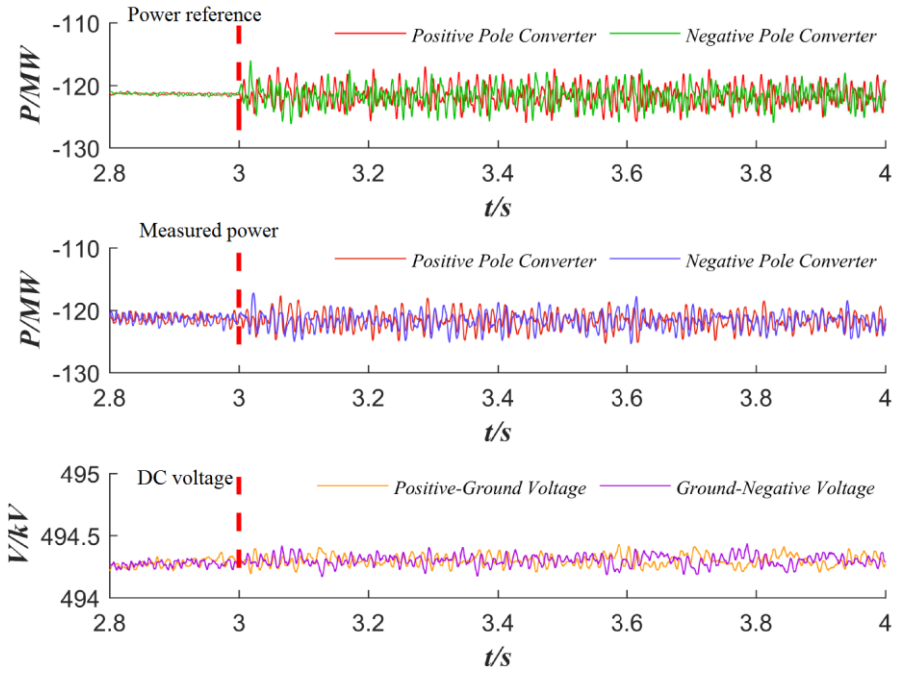

Fig. 6 The simulation results of the power reference, measured power, and dc voltage for the conventional linear droop control with *k* changed from 5 to 40.

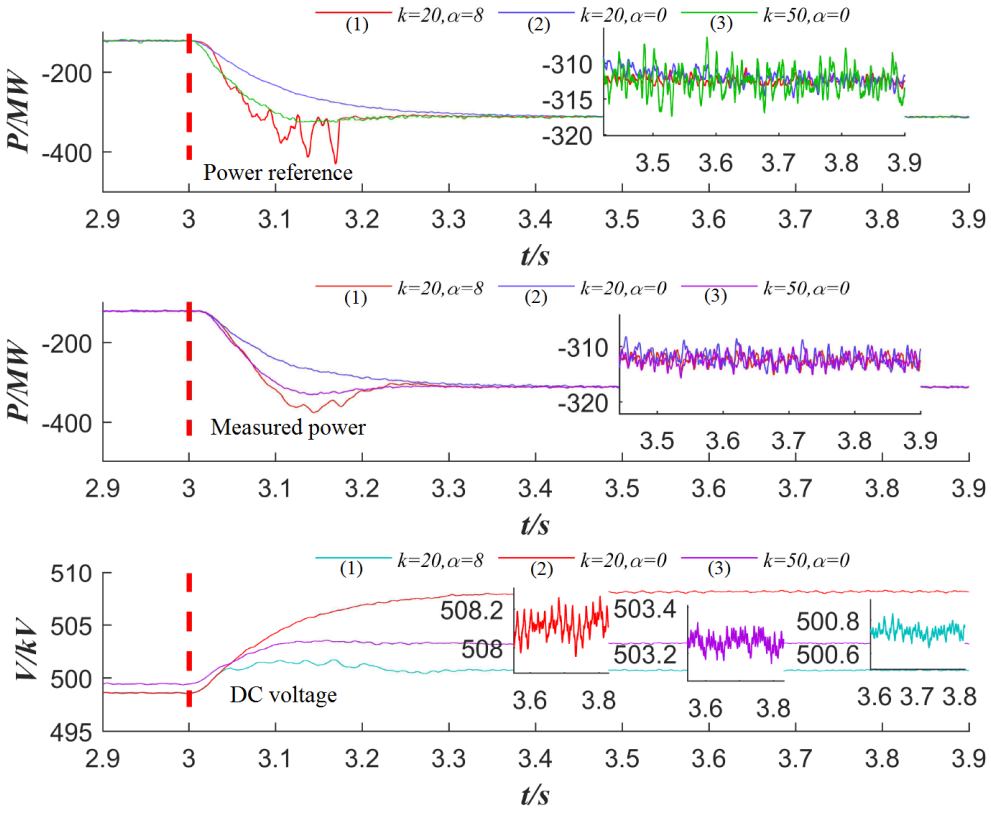

Fig. 7 The simulation results of the power reference, measured power, and dc voltage for (1) the proposed droop (k = 20, α = 8), (2) the linear droop control with the steep slop (k = 20, α = 0), and (3) the linear droop control with the shallow slop (k = 50, α = 0).

4.3 Performance of the Proposed Hybrid Droop with Self-Correction Algorithm

As aforementioned, the regulation speed and voltage deviation of the conventional nonlinear droop are affected by operating point moving. Figure 8 shows the power reference, measured power, and dc voltage for the proposed droop with and without the reference self-correction algorithm by using k = 20 and α = 8. In Fig. 8, the dynamic performance during two regulations shows that the performance of the nonlinear droop is influenced by moving operating point and there is stability issue. The hybrid droop control with the reference self-correction algorithm can ensure that every regulation will have same performance on regulation speed and voltage deviation, and can improve system stability.

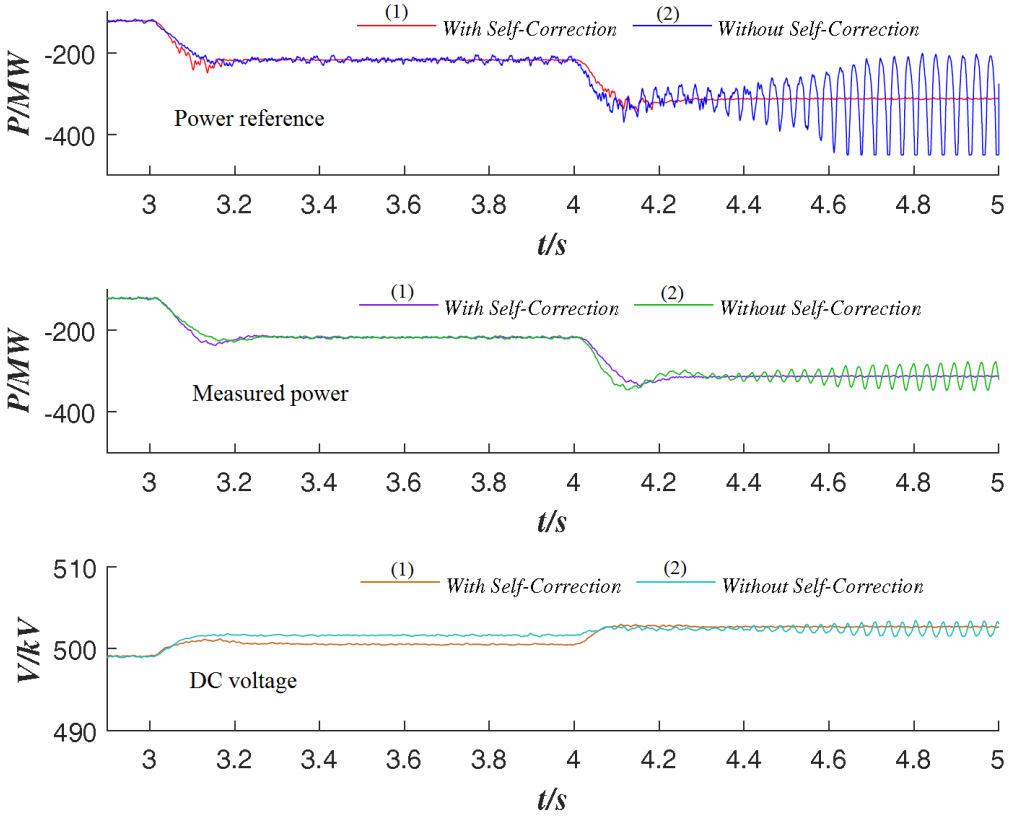

Fig. 8 The simulation results of the power reference, measured power, and dc voltage for the proposed droop control (1) with reference self-correction and k = 20, α = 8, (2) without reference self-correction and k = 20, α = 8.

5. Conclusion

The conventional linear droop with the shallow slope can achieve fast regulation speed and small voltage deviation but large ripple in power and voltage. The conventional nonlinear droop control has different performance for different operating points, which may cause system instability under certain conditions. In this paper, a hybrid droop control with a cubic acceleration term and reference self-correction algorithm is proposed for VSC-MTDC system. The proposed droop control has fast regulation speed and low voltage deviation during a transient due to its nonlinear characteristics. The developed reference self-correction algorithm can move the droop curve to the new operating point for eliminating voltage deviation and reducing voltage and power ripples, thereby improving system dynamic response and stability.

References

[1] K. Rouzbehi, A. Miranian, J. I. Candela, A. Luna, and P. Rodriguez, "A generalized voltage droop strategy for control of multiterminal dc grids," IEEE Transactions on Industry Applications, vol. 51, no. 1, pp. 607-618, 2015.

[2] K.-J. Li, J.-g. Ren, L.-J. Sun, J.-g. Zhao, Y.-L. Liang, W.-J. Lee, Z.-h. Ding, Y. Sun et al., "A coordination control strategy of voltage-sourceconverter-based mtdc for offshore wind farms," IEEE Transactions on Industry Applications, vol. 51, no. 4, pp. 2743-2752, 2015.

[3] P. Li, W. Wang, X. Yang, S. Wang, H. Cui, and C. Gao, "A droop control method of microsources based on divided self-adjusting slope coefficient," in Power System Technology (POWERCON), 2010 International Conference on. IEEE, 2010, pp. 1-6.

[4] C. Wang, J. Meng, Y. Wang, and H. Wang, "Adaptive virtual inertia control for dc microgrid with variable droop coefficient," in Electrical Machines and Systems (ICEMS), 2017 20th International Conference on. IEEE, 2017, pp. 1-5.

[5] Q. Tran, H. Shehadeh, E. R. Sanseverino, S. Favuzza, and M. Di Silvestre, "Nonlinear droop control for minimum power losses operation in islanded microgrids," in Environment and Electrical Engineering and 2017 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I&CPS Europe), 2017 IEEE International Conference on. IEEE, 2017, pp. 1-5.

[6] P. Prabhakaran, Y. Goyal, and V. Agarwal, "Novel nonlinear droop control techniques to overcome the load sharing and voltage regulation issues in dc microgrid," IEEE Transactions on Power Electronics, vol. 33, no. 5, pp. 4477-4487, 2018.

[7] Y. Li, G. Tang, J. Ge, Z. He, H. Pang, J. Yang, and Y. Wu, "Modeling and damping control of modular multilevel converter based dc grid," IEEE Transactions on Power Systems, vol. 33, no. 1, pp. 723-735, 2018.

Part III

Feedforward Accurate Power Sharing and Voltage Control for Multi-Terminal HVDC Grids

Ali Mehrizi-Sani
Armin Teymouri

Washington State University

For information about this project, contact

Ali Mehrizi-Sani
Washington State University
School of Electrical Engineering and Computer Science
Pullman, WA 99163
Phone: 509-432-5989
Email: mehrizi@wsu.edu

Power Systems Engineering Research Center

The Power Systems Engineering Research Center (PSERC) is a multi-university Center conducting research on challenges facing the electric power industry and educating the next generation of power engineers. More information about PSERC can be found at the Center's website: http://www.pserc.org.

For additional information, contact:

Power Systems Engineering Research Center
Arizona State University
527 Engineering Research Center
Tempe, Arizona 85287-5706
Phone: 480-965-1643
Fax: 480-727-2052

Notice Concerning Copyright Material

Table of Contents

1. Introduction 2
2. MTDC Study System Modeling and Control 3
    2.1 AC Network Model 4
    2.2 Droop-Based DC Voltage and Real Power Controller 4
    2.3 Proposed Feedforward Loop 5
3. Simulation Results 6
    3.1 Accurate Power Sharing between Converters 6
    3.2 DC-Side Voltage Control 6
    3.3 Response to AC-Side Load Change 8
4. Conclusion 12
References 13

List of Figures

Figure 1 Four-bus MTDC study system 3

Figure 2. Proposed model of a converter station with droop-based voltage and power controller 4

Figure 3. Droop characteristics of two converter stations 5

Figure 4. Real powers of the converters as a result of a change in $P_{ref,1}$ 6

Figure 5. DC-side voltages of the converters as a result of a change in $P_{ref,1}$ 7

Figure 6. DC-side voltages of the converters as a result of a change in their references values 7

Figure 7. Real powers of the converters as a result of a change in the DC-side voltages 7

Figure 8. Real powers of the converters with a load added to AC-side of terminal 3 using (a) the conventional method, (b) the proposed feedforward method with droop gains 8

Figure 9. DC voltages of the converters with a load added to the AC-side of terminal 3 using (a) the convetional method, (b) the proposed feedforward method with droop gains 9

List of Tables

Table 1. Parameters of the study system..... 9

1. Introduction

Multi-terminal direct current (MTDC) systems are a potentially feasible solution, both economically and technically, for the integration of renewable energy sources and the connection of different AC grids with different frequencies [1]. Voltage-sourced converters (VSC) and line-commutated converters (LCC) are two common power converters used in MTDC systems [2]. Several advantages of VSC over LCC, such as independent and flexible real and reactive power control, black start capability, no commutation failure, and smaller footprint, have made the VSC-based MTDC a dominant solution [3]. However, there are still challenges regarding DC voltage regulation and power flow control in the operation of VSC-MTDC systems [4].

Different methods are proposed to control the voltage and power in MTDC systems [5–8]. The most common method to control the DC-side voltages is the master-slave control [5, 6]. In this method, one converter is responsible for the voltage control while other converters control their power [7, 8]. However, this method has a low reliability since a single failure can corrupt the voltage regulation. It also relies on fast communication of the remotely measured signals to the master converter.

Voltage droop is an alternative to master-slave control. Voltage droop distributes the voltage regulation responsibility between several converters while the power is controlled by the remaining converters based on their droop coefficients [9, 10]. However, this method has some disadvantages such as the DC-side voltage imbalance [11], overloading in converters [12], and instability caused by load changes on the AC side.

Different aspects of MTDC systems have been investigated in the literature. Reference [13] discusses an adaptive droop-based power sharing strategy for MTDC systems with off-shore wind farms. This strategy needs to be updated whenever the topology of the system changes. A droop-based control strategy that is independent of the DC system topology and line parameters is investigated in [14]. Reference [15] studies an autonomous voltage droop-based coordination of VSC stations in an MTDC system without the need for communication. Reference [16] proposes a model predictive controller (MPC) to coordinate the voltage droop coefficients in an MTDC. Reference [17] proposes an approach for a generalized power flow in a VSC-based MTDC grid. A coordination strategy for the secondary and primary voltage and frequency controllers in an MTDC grid is developed in [18]. Power sharing between different VSC stations is investigated in [19]. References [20] propose a method to damp interarea oscillations using a multi-input multi-output controller. A power reduction-based scheme to prevent DC overvoltages is proposed in [21]. Reference [22] reviews different modeling, control, and protection techniques available for MTDC grids.

Although extensive research studies are performed on MTDC voltage control, to the best of the authors' knowledge, none of them addresses the inaccuracies in the DC voltage regulation and power sharing caused by a load change on the AC-side terminal. To mitigate this shortcoming, this project proposes an improved voltage regulation and accurate power sharing scheme that, unlike the available literature [14, 15], can maintain the desired voltage and power values after a large load is added to the AC terminals of the MTDC converters. The proposed method is implemented using a generalized droop-based controller.

The remainder of this report is organized as follows. Section II illustrates the proposed MTDC study system. This section develops the DC and AC network models and explains the design process of the controllers. The proposed feedforward controller is also presented in this section. Section III reports the simulation results. The conclusions are provided in Section IV.

2. System Modelling and Control

The topology of an MTDC network varies depending on different factors such as geographical concerns, economical conditions, and technical issues [6]. In this project, to analyze the effectiveness of the proposed control strategy, the four-bus test system shown in Fig. 1 is utilized. The DC network connects the AC grids through π section transmission lines that have different impedance and admittance values based on their lengths. The power converters used to connect the AC grid to the DC network are bidirectional. Power input converters are used when there is a power source, such as an off-shore wind farm, on the AC side, while power output converters are connected to AC power grids [6].

To model the DC network, a generalized π section of the transmission line and its equations are used [14]. Using a π section instead of a resistance makes the analysis valid for transients as well. In Fig. 1, Z_1 to Z_5 are the DC cable impedances, Y_1 to Y_5 are the DC cable admittances, I_{DC1} to I_{DC5} are the DC line currents, and V_{DC1} to V_{DC4} are the voltages of the DC-side capacitors. This section develops the equations of the DC network by assuming I_{DC1}, I_{DC2}, I_{DC3}, and V_{DC4} as inputs. These equations are derived by finding the relationship between the DC-side voltages and currents.

$$V_{DC1} = V_5 \frac{Z_1 Y_1}{2} + I_{DC1} Z_1 \tag{1}$$

$$V_{DC2} = V_5 \frac{Z_2 Y_2}{2} + I_{DC2} Z_2 \tag{2}$$

$$V_{DC3} = V_6 \frac{Z_3 Y_3}{2} + I_{DC3} Z_3 \tag{3}$$

$$V_{DC4} = V_6 \frac{Z_4 Y_4}{2} + I_{DC4} Z_4 \tag{4}$$

$$V_5 = V_6 \frac{Z_5 Y_5}{2} + I_{DC5} Z_5 \tag{5}$$

$$I_{DC5} = I_{DC1} + I_{DC2} = -I_{DC3} - I_{DC4} \tag{6}$$

Using these equations, the MTDC system equations are derived as shown in (7). The power flow equation for the MTDC system i ($i = 1, ..., 4$) is derived as follows:

$$P_i = V_{DCi} I_{DCi} \tag{8}$$

2.1 AC Network Model

The converters are modeled in the dq reference frame, as seen in Fig. 2. The dq modeling allows for the decoupled control of real and reactive currents in each converter. DC-side voltage and real power are controlled by the d-axis current while AC-side voltage and reactive power are controlled

by the q-axis currents of the converters. The AC-side equations of the converters in the dq reference frame are as follows [23]:

$$v_{t,d} = R_f i_d + L_f \frac{di_d}{dt} + v_{s,d} - L_f \omega i_q, \tag{9}$$

$$v_{t,q} = R_f i_q + L_f \frac{di_q}{dt} + v_{s,q} + L_f \omega i_d \tag{10}$$

2.2 Droop-Based DC Voltage and Real Power Controller

Fig. 2 shows the control block diagram of each converter. The reference value for the d-axis current is derived by the outer loop of the hierarchical controller (i.e., the droop-based voltage and power controller). The droop-based controller is expressed as follows:

$$V_{DC} + kP + a = 0. \tag{11}$$

Ceofficients k and a depend on the voltage and power characteristics of the converters and their AC systems. The value of $|a|$ equals the nominal value of the DC voltage when the real power is not transferred by the VSC. k is the slope of the voltage droop characteristic, which is determined based on the relationship between different converters, as will be discussed later in this section. Fig. 3 shows the droop characteristics of a single converter. According to (8), with the DC-side voltage being constant, the real power is proportional to the DC-side current. As seen in Fig. 1, VSC$_i$ and VSC$_{i+1}$ are power input converters, for $i = 1$, and power output converters, for $i = 3$. Using (8), with V_{DC} values being the same, the real powers of the VSCs can be controlled with the ratio of $c = \frac{P_i}{P_{i+1}} = \frac{I_{DC,i}}{I_{DC,i+1}}$.

The reference d-axis current is calculated as

$$i_{d,ref} = (k_p + \frac{k_i}{s})(V_{DC} - [V_{DC,\text{ref}} - D_i \frac{G}{1+Ts}(P_{i,\text{ref}} - P_i)]. \tag{12}$$

Considering $\Delta P_i = P_i - P_{i,ref}$ and $\Delta V_{DC} = V_{DC} - V_{DC,ref}$ as the inputs of the system, (12) can be rewritten as

$$i_{d,ref} = (k_p + \frac{k_i}{s})\Delta V_{DC} - \frac{GD_i}{1+Ts}(k_p + \frac{k_i}{s})\Delta P_i. \tag{13}$$

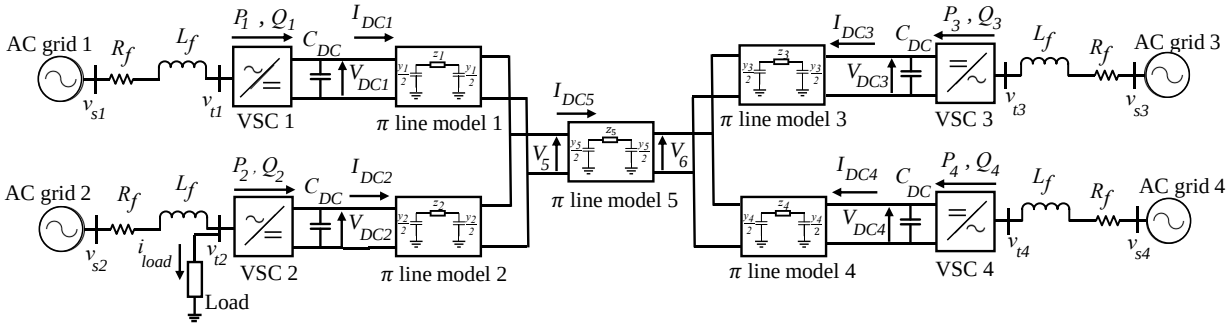

Figure 1: Four-bus MTDC study system.

$$\begin{bmatrix} V_{DC1} \\ V_{DC2} \\ V_{DC3} \\ I_{DC4} \end{bmatrix} = \begin{bmatrix} Z_1 + \frac{Z_1}{Y_1}(Z_5 + \frac{Z_5 Y_5}{Y_4}) & \frac{Z_1 Y_1 Z_5}{2} & 0 & \frac{Z_1 Y_1 Z_5 Y_5}{2 Z_4 Y_4} \\ \frac{Z_2 Y_2 Z_5}{2} + \frac{Z_2 Y_2 Z_5 Y_5}{2 Y_4} & Z_2 + \frac{Z_2 Y_2 Z_5}{2} + \frac{Z_2 Y_2 Z_5 Y_5}{2 Y_4} & \frac{Z_2 Y_2 Z_5 Y_5}{2} & 0 \\ \frac{Z_3 Y_3}{Y_4} & \frac{Z_3 Y_3}{Y_4} & Z_3 + \frac{Z_3 Y_3}{Y_4} & \frac{Z_3 Y_3}{Z_4 Y_4} \\ -1 & -1 & -1 & 0 \end{bmatrix} \begin{bmatrix} I_{DC1} \\ I_{DC2} \\ I_{DC3} \\ V_{DC4} \end{bmatrix}. \quad (7)$$

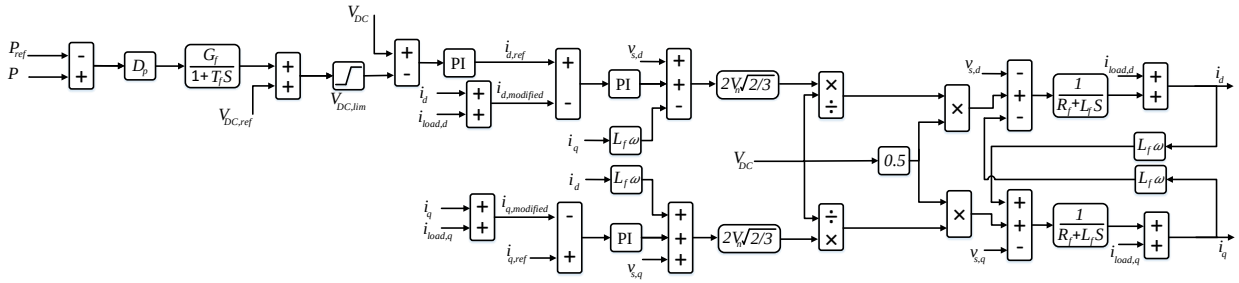

Figure 2: Proposed model of a converter station with droop-based voltage and power controller.

The outer loop of the proposed controller needs to be slower than the inner loop. Thus, a low pass filter is used in the outer loop. Equation (13) shows that this filter adds a negative pole ($\frac{-1}{T}$) to the transfer function of the studied multi-input-single-output (MISO) controller, which decreases the steady state oscillations.

Based on (1), (2), and (7), the changes in the DC-side currents of VSC$_i$ and VSC$_{i+1}$, $i = 1, 3$, can be expressed as

$$\Delta I_{DC,i} = k_i \frac{Z_i Y_i}{2} \Delta V_{5(6)} + k_i Z_i \Delta I_{DC,i} \quad (14)$$

$$\Delta I_{DC,i+1} = k_{i+1} \frac{Z_{i+1} Y_{i+1}}{2} \Delta V_{5(6)} + k_{i+1} Z_{i+1} \Delta I_{DC,i+1} \quad (15)$$

where ΔV_5 is used for $i = 1$ and ΔV_6 for $i = 3$. The relationship between $\Delta i_{DC,i}$ and $\Delta i_{DC,i+1}$ is determined by (14) and (15) based on the real power transmission ratio c, which is set by the system operator. Thus, the relationship between the slope of the droop characteristics of VSC$_i$ and VSC$_{i+1}$ can be found using (14), (15) as

$$k_{i+1} = \frac{k_i Z_i Y_i}{Z_{i+1} Y_{i+1} c + k_i Z_i Z_{i+1} Y_i - k_i Z_i Z_{i+1} Y_{i+1} c}. \quad (16)$$

2.3 Proposed Feedforward Loop

Apart from a power sharing and voltage control algorithm, an MTDC network should be able to continue its normal operation when disturbances happen on the AC sides of the VSCs. None of the proposed power sharing algorithms considers the effects of an added AC load on the real powers and

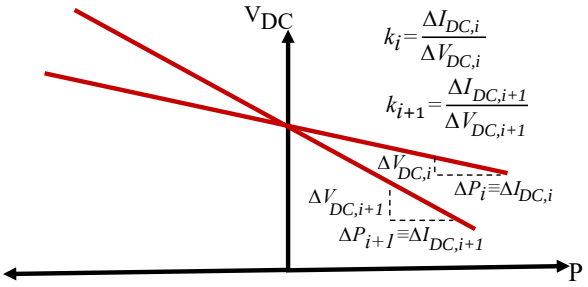

Figure 3: Droop characteristics of two converter stations.

DC voltages of an MTDC network [6, 14, 15]. This load can cause unwanted reverse power flows through the VSCs, as will be shown in Section III, as well as a significant drop in DC voltages.

Adding a feedforward signal containing the d- and q- axes of the load current cancels the effect of the load current on the VSC current controller. This enables the MTDC network controllers to maintain their real power and DC voltage set points. Fig. 2 shows the proposed feedforward loop, as it is subtracted from the current controller input and added to the output current within the AC grid model.

3. Simulation Results

This section evaluates the performance of the proposed scheme and compares it with the traditional control methods using different case studies performed in the PSCAD/EMDTC software by studying the four-bus MTDC system in Fig. 1. Bus 4 works as the slack bus and controls the DC-side voltages of all the buses. As a result, based on (11), k_4 is zero. The other buses are responsible for real and reactive power control and work in PQ mode with identical nonzero k coefficients. The converters located at buses 1 and 2 work as power input converters and the converter at bus 3 works as a power output converter. The parameters of the system are shown in Table I.

3.1 Accurate Power Sharing Between Converters

To show the capability of the proposed system in controlling and accurately sharing the real powers, the PQ buses are set to transfer certain amounts of real power, $P_1 = 0.2$ MW, $P_2 = 0.3$ MW, and $P_3 = -0.5$ MW. Bus 4 is responsible for DC voltage control with the set point of 1 kV. At $t = 0.7$ s, the real power reference of bus 3 is changed from 0.2 MW to 0.4 MW. Fig. 4 shows how P_1 tracks its reference while the other PQ converters maintain their real powers. The change in P_4 is to control the DC-side voltages and maintain the real power balance in the DC network. P_4 also represents the real power loss in the DC network that is lower than 3%. Fig. 5 shows the DC-side voltages as a result of the power set point change. The steady state voltages remain at their set points although the real power set point is changed.

3.2 DC-Side Voltage control

This case study shows the capability of the proposed controller in regulating the DC-side voltages independently of the real powers. While the PQ buses are transferring certain amounts of real power, $P_1 = 0.2$ MW, $P_2 = 0.3$ MW, and $P_3 = -0.5$ MW, at $t = 0.7$ s, the DC voltage set point changes from 1.0 kV to 0.9 kV. It returns to its initial value of 1.0 kV at $t = 1.0$ s. Fig. 6 shows how the DC-side voltages track their reference values. The real powers of different buses are shown in Fig. 7. The VSCs maintain their real power set points when the DC voltages change.

3.3 Response to AC-Side Load Change

This section evaluates the effectiveness of the added feedforward loop by comparing the performance of the system with and without the proposed method to a change in the AC-side load. The DC-side voltage and the real power set points of all the converters remain constant during this case study. At $t = 0.7$ s, a 3 MW load is switched on at the AC-side terminal of the converter in bus 3. Fig. 8(a) shows that real power of the converters using the conventional method cannot maintain their set points after the load is added. Fig. 8(b) shows the real powers in the droop-based system with the feedforward controller. Using the feedforward loop allows the converters to operate independently of the disturbances on their AC sides. Therefore, these disturbances are picked up by the AC grid, not the MTDC system.

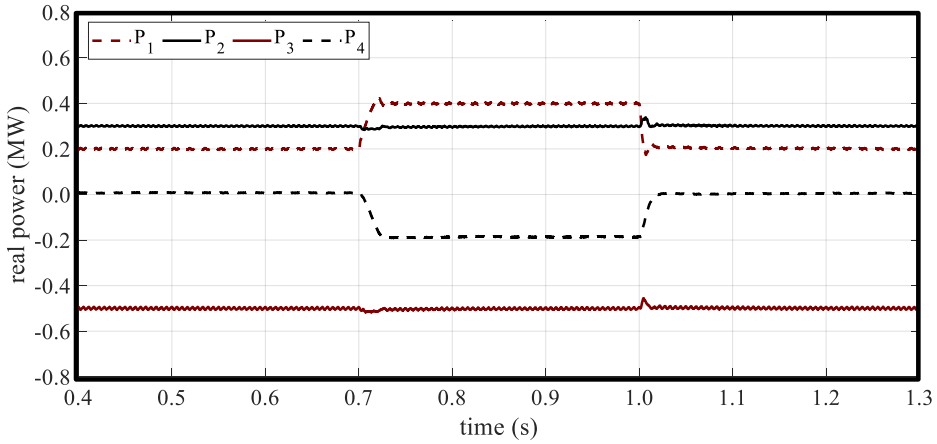

Figure 4: Real powers of the converters as a result of a change in P_{ref1}.

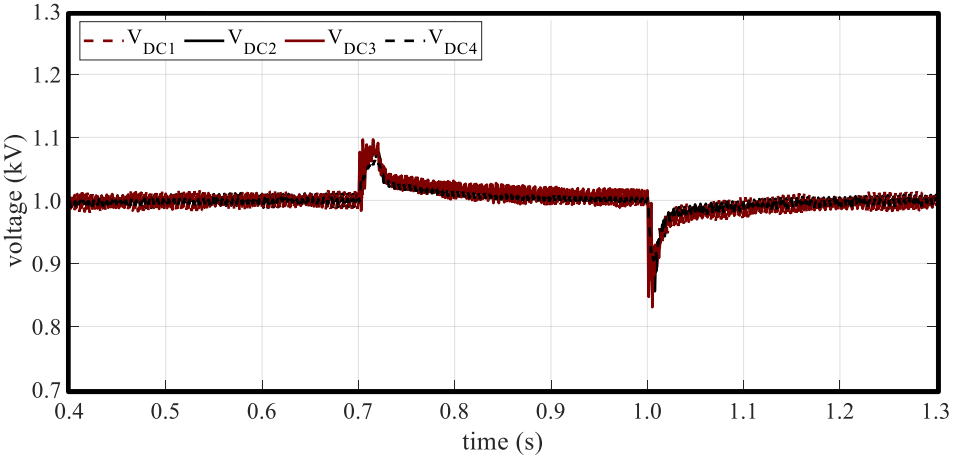

Figure 5: DC-side voltages of the converters as a result of a change in $\text{P}_{\text{ref,1}}$.

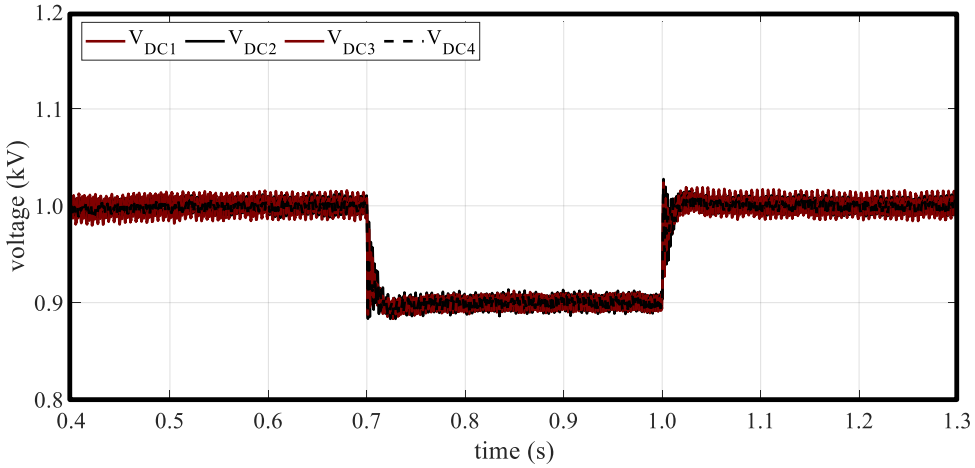

Figure 6: DC-side voltages of the converters as a result of a change in their reference values.

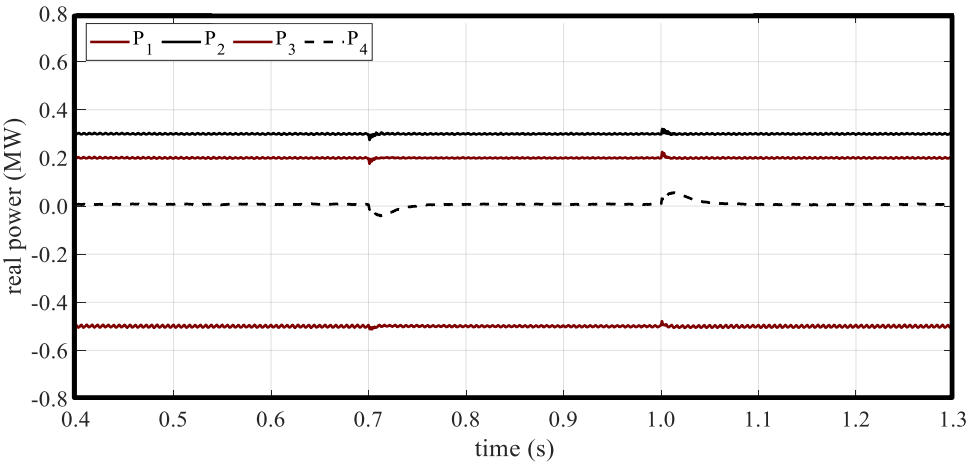

Figure 7: Real powers of the converters as a result of a change in the DC-side voltages

Fig. 9 shows the DC-side voltages as a result of the load change. Fig. 9(a) shows that the conventional controller cannot keep the DC-side voltages on their references when the load changes. All the DC-side voltages drop to lower than the permitted voltage deviation (5%). Thus, the system cannot continue its normal operation. Fig. 9(b) shows that the proposed scheme can keep the DC-side voltages on the desired value.

Table 1: Parameters of the study system.

Grid-Connected VSC Parameters			
$V_{s,rms}$	480 V	C_{DC}	4 mF
f_s	60 Hz	L_f	50 µH
$f_{\text{switching}}$	2.63 kHz	R_f	11 $m\Omega$
Control Parameters			
Current Controller		Voltage Controller	
K_p	0.200	K_p	8.000
T_i	0.005	T_i	0.010
DC Lines Parameters			
	Resistance	Inductance	Capacitance
π section 1	2.9 mΩ	1.4 mH	0.1 µF
π section 2	2.9 mΩ	1.4 mH	0.1 µF
π section 3	3.0 mΩ	2.8 mH	0.2 µF
π section 4	3.0 mΩ	2.8 mH	0.2 µF
π section 5	3.2 mΩ	3.0 mH	0.3 µF

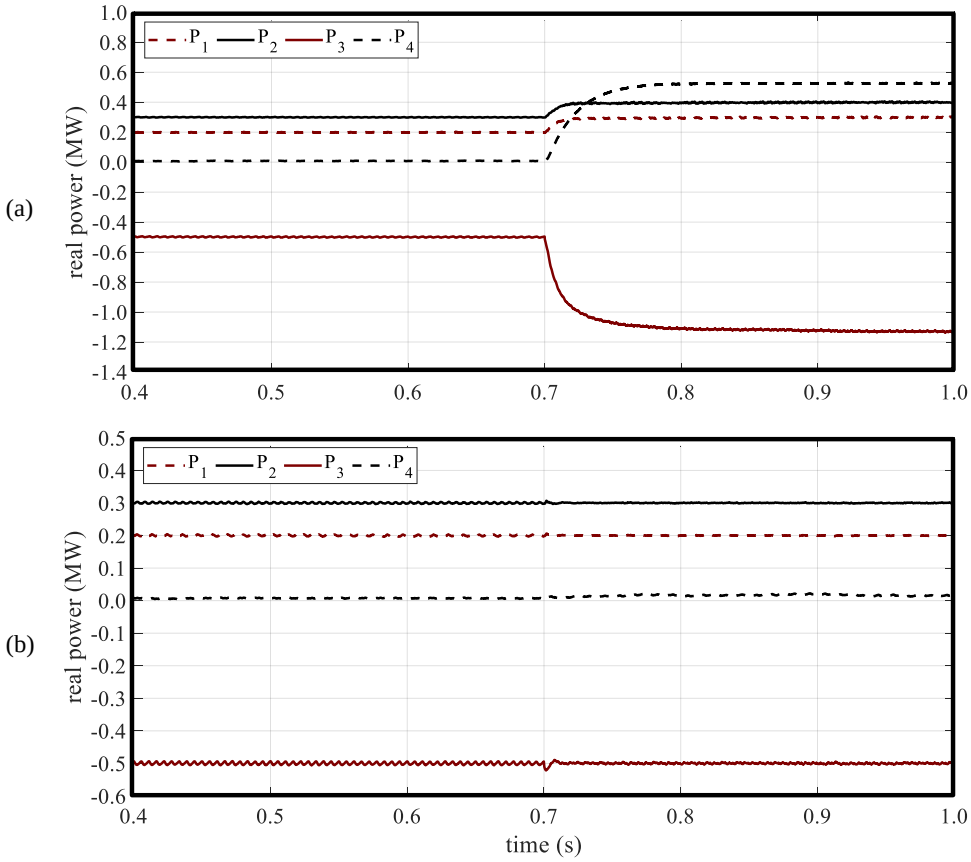

Figure 8: Real powers of the converters with a load added to the AC-side of terminal 3 using (a) the conventional method, (b) the proposed feedforward method with droop gains.

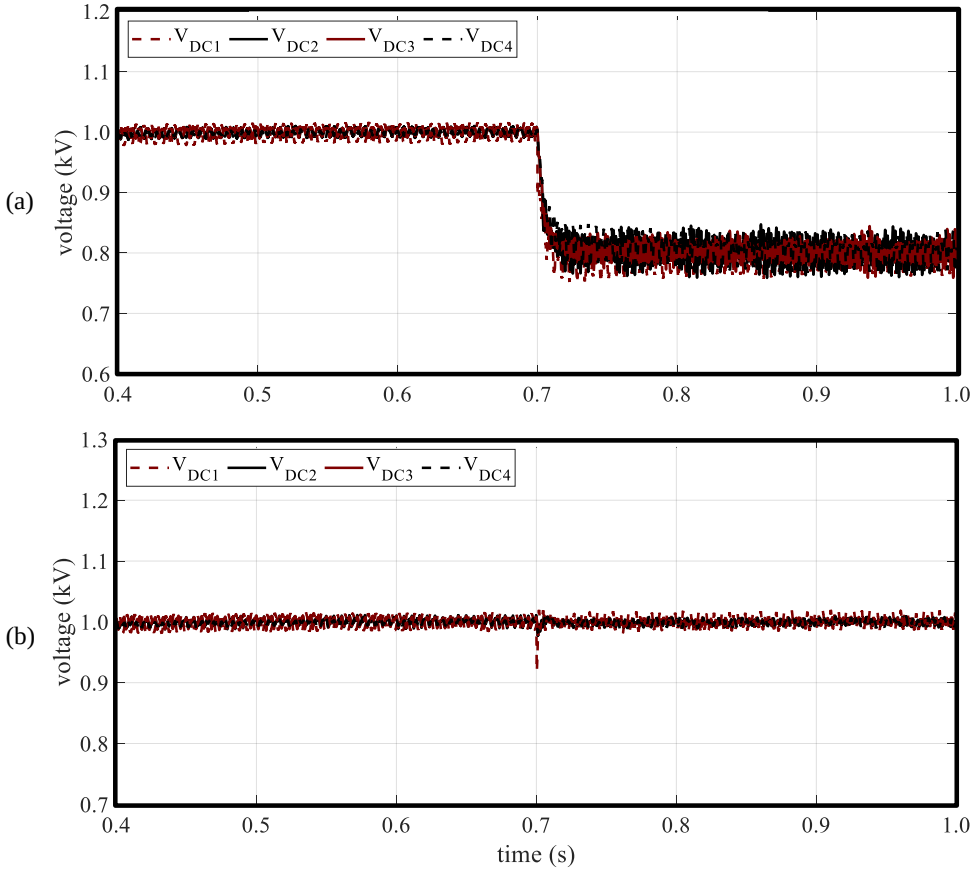

Figure 9: DC voltages of the converters with a load added to the AC-side of terminal 3 using (a) the conventional method, (b) the proposed feedforward method with droop gains.

4. Conclusion

This project proposes a generalized P-V droop-based control strategy for accurate power sharing and voltage regulation in MTDC systems. A DC grid with four terminals is used to validate the effectiveness of the proposed scheme after a complete mathematical justification. It is shown that the proposed scheme can track the power reference changes in VSC units while keeping the voltages within the desired thresholds. Furthermore, the advantages of the proposed feedforward scheme over conventional controllers is demonstrated during demand changes on the AC grids. Unlike the conventional MTDC controllers, the proposed control scheme can maintain accurate power sharing and voltage control when AC-side demand changes.

References

[1] W. Zhang, K. Rouzbehi, J. Candela, A. Luna, G. B. Gharehpetian, and P. Rodriguez, "Autonomous interia-sharing control of multi-terminal VSC-HVDC grids," in *IEEE Power Energy Soc. General Meeting*, Jul. 2016.

[2] O. D. Adeuyi, M. Cheah-Mane, J. Liang, L. Livermore, and Q. Mu, "Preventing dc over-voltage in multi-terminal HVDC transmission," *CSEE J. Power Energy Syst*., vol. 1, no. 1, May. 2015.

[3] L. Xiao, Z. Xu, T. An, and Z. Bian, "Improved analytical model for the study of steady state performance of droop-controlled VSC-MTDC systems," *IEEE Trans. Power Syst*., vol. 32, no. 3, pp. 2083-2093, Aug. 2017.

[4] W. Lu and B.-T. Ooi, "Premium quality power park based on multi-terminal HVDC," *IEEE Trans. Power Del*., vol. 20, no. 2, pp. 978-983, Apr. 2005.

[5] N. Bayati, A. Hajizadeh, and M. Soltani, "Impact of faults and protection methods on DC microgrids operation," in *Int. Conf. Envi. Electr. Eng. and Ind. Commercial Power Syst. Europe*, Jun. 2018.

[6] M. A. Abdelwahed and E. F. El-Saadany, "Power sharing control strategy of multiterminal VSC-HVDC transmission systems utilizing adaptive voltage droop," *IEEE Trans. Sustainable Energy*, vol. 8, no. 2, pp. 605-615, 2017.

[7] M. Kermani, "Transient voltage and frequency stability of an isolated microgrid based on energy storage systems," in *IEEE Int. Conf. Envi. Electr. Eng*., Jun. 2016.

[8] A. Teymouri, S. H. Fathi, and F. Karbakhsh, "An advanced hysteresis controller to improve voltage profile of power system with pv units: A smart grid power exchange framework," in *IEEE Int. Power Syst. Conf*., Nov.

[9] N. R. Chaudhuri and B. Chaudhuri, "Adaptive droop control for effective power sharing in multi-terminal dc (mtdc) grids," *IEEE Transactions on Power Systems*, vol. 28, no. 1, pp. 21-29, 2013.

[10] M. Mousavi, A. Mehrizi-Sani, D. Ramasubramanian, and E. Farantatos, "Performance evaluation of an angle droop-based power sharing algorithm for an inverter-dominated power system," Aug. 2019.

[11] N. Bayati, A. Hajizadeh, and M. Soltani, "Protection in dc microgrids: a comparative review," *IET Smart Grid*, vol. 1, no. 3, pp. 66-75.

[12] G. Parise, L. Martirano, M. Kermani, and M. Kermani, "Designing a power control strategy in a microgrid using pid/fuzzy controller based on battery energy storage," in *IEEE Int. Conf. Environment Electr. Engineering and IEEE Ind. Commercial Power Syst. Europe (EEEIC/I&CPS Europe).* IEEE, 2017, pp. 1-5.

[13] M. A. Abdelwahed and E. F. El-Saadany, "Power sharing control strategy of multiterminal vsc-hvdc transmission systems utilizing adaptive voltage droop," *IEEE Trans. Sustain. Energy*, vol. 8, no. 2, pp. 605-612, Sept. 2017.

[14] A. Kirakosyan, E. F. El-Saadany, M. S. El Moursi, S. Acharya, and K. Al Hosani, "Control approach for the multi-terminal HVDC system for the accurate power sharing," *IEEE Trans. Power Syst.*, vol. 33, no. 4, pp. 4323-4334, 2018.

[15] A. Raza, Y. Liu, K. Rouzbehi, M. Jamil, S. O. Gilani, X. Dianguo, and B. W. Williams, "Power dispatch and voltage control in multiterminal hvdc systems: A flexible approach," *IEEE Access*, vol. 5, pp. 24608-24616, 2017.

[16] G. Li, Z. Du, C. Shen, Z. Yuan, and G. Wu, "Coordinated design of droop control in MTDC grid based on model predictive control," *IEEE Trans. Power Syst*., vol. 33, no. 3, pp. 2816-2828, 2018.

[17] J. Lei, T. An, Z. Du, and Z. Yuan, "A general unified AC/DC power flow algorithm with MTDC," *IEEE Trans. Power Syst*., vol. 32, no. 4, pp. 2837-2846, 2017.

[18] C. Gavriluta, I. Candela, A. Luna, A. Gomez-Exposito, and P. Rodriguez, "Hierarchical control of HV-MTDC systems with droop-based primary and OPF-based secondary," *IEEE Trans. Smart Grid*, vol. 6, no. 3, pp. 1502-1510, 2015.

[19] K.-J. Li, J.-g. Ren, L.-J. Sun, J.-g. Zhao, Y.-L. Liang, W.-J. Lee, Z.-h. Ding, Y. Sun *et al*., "A coordination control strategy of voltage-source-converter-based MTDC for offshore wind farms," *IEEE Trans. Ind. Appl*., vol. 51, no. 4, pp. 2743-2752, 2015.

[20] A. Banerjee, N. R. Chaudhuri, and R. G. Kavasseri, "A novel explicit disturbance model-based robust damping of interarea oscillations through MTDC grids embedded in AC systems," *IEEE Trans. Power. Del.*, vol. 33, no. 4, pp. 1864-1874, 2018.

[21] O. D. Adeuyi, M. Cheah-Mane, J. Liang, L. Livermore, and Q. Mu, "Preventing dc over-voltage in multi-terminal HVDC transmission," *CSEE J. Power Energy Syst.*, vol. 1, no. 1, pp. 86-94, 2015.

[22] L. Zhang, Y. Zou, J. Yu, J. Qin, V. Vittal, G. G. Karady, D. Shi, and Z. Wang, "Modeling, control, and protection of modular multilevel converter-based multi-terminal HVDC systems: A review," *CSEE J. Power energy Syst.*, vol. 3, no. 4, pp. 340-352, 2017.

[23] P. M. Shabestari, S. Ziaeinejad, and A. Mehrizi-San, "Reachability analysis for a grid-connected voltage-sourced converter (VSC)," in IEEE Applied Power Electron. Conf. Expo. (APEC), Mar. 2018.