



Efficient Modeling of Modular Multilevel Converters for Fast Simulation of Large-Scale MMC-HVDC Embedded Power Systems

Final Project Report

S-78G

Power Systems Engineering Research Center
*Empowering Minds to Engineer
the Future Electric Energy System*



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Executive Summary

Modular multilevel converter (MMC) has become the most attractive multilevel converter topology for voltage-sourced converter high-voltage direct current (VSC-HVDC) transmission systems. The salient features of MMC include: 1) modularity and scalability to meet any voltage level by stacking up additional numbers of SMs without increasing topology complexity, 2) inherent redundancy and fault-tolerance capability to improve reliability, 3) high efficiency suitable for high-power applications, and 4) high power quality and low filter/transformer cost due to filter-free and transformerless applications by realization of high-level converters. With the increasing number of the MMC-HVDC systems embedded into ac grids, the performance of the present power systems may be dramatically improved, including stability, reliability, capacity, and efficiency. However, the MMCs' applications are restricted due to several important technical challenges. One of the major challenges is to effectively and accurately model various MMCs for fast simulation of large-scale power systems. In this report, an equivalent circuit model (ECM) is proposed for modeling and simulating the MMCs based on various submodule (SM) circuits and arm configurations. The proposed ECM can significantly improve simulation efficiency and be applied for precharging, normal, and fault operation analysis of the MMC-HVDC systems while considering the behaviors of various SM circuits. The proposed accelerated model can also be used to investigate internal dynamics with various control strategies, e.g., capacitor voltage balancing, when full states are considered. To further improve efficiency, the proposed model can be implemented by the reduced-order algorithm. The effectiveness of the proposed ECM is verified by an MMC-HVDC system built in PSCAD/EMTDC software environment. Also, the proposed ECM is applicable for other simulation platforms.

Problems of the Existing Models

The MMC with half-bridge (HB) SMs is the dominant topology for HVDC systems due to its low cost and low loss. However, in case of a dc-side short-circuit fault, the HB-MMC cannot block the fault currents fed from ac grid. Therefore, various SMs have been proposed and investigated to improve the fault blocking capability of the MMCs, such as the full-bridge (FB), unipolar-voltage full-bridge (UFB), clamp-double (CD), and three-level/five-level cross-connected (3LCC/5LCC) SMs. These fault-blocking SMs can block the fault current fed from ac grids. For large-scale MMCs-embedded power systems, it is required to investigate dynamic performance, fault, protection, and stability. The conventional detailed switching model (DSM) is time consuming and infeasible due to the large number of semiconductor switches in high-level systems. To address this challenge, several MMC models have been developed to accelerate the electromagnetic transient (EMT) simulation. However, the existing models are usually developed for some specific SM circuits and certain operating conditions. They also do not consider bipolar arm voltages and static compensator (STATCOM) operating conditions during a fault.

The Proposed Equivalent Circuit for Modeling the MMCs

To consider various SM circuits and different operating conditions, a generalized equivalent circuit of an arm of the MMC is proposed. The proposed equivalent arm circuit consists of a controllable voltage source, four controllable switches, and four diodes. By properly switching

on and off the four switches, the proposed circuit can simulate the behaviors of various SM circuits, i.e., the HB, FB, UFB, CD, 3LCC, and 5LCC SMs under different operating conditions, including startup, normal, and fault operations. Therefore, based on the proposed equivalent arm circuit, the MMCs with various configurations can be modeled in a general way and simulated for efficiently analyzing large-scale hybrid ac and dc power systems.

In this study, several operating conditions will be considered, including precharging/startup condition, normal, and fault conditions. Under the precharging/startup condition, the SM capacitors will be charged to the nominal voltage. For normal operation, the internal dynamics of the MMCs should be controlled properly. During a dc fault, all semiconductor switches of the MMCs are turned off; the HB SM cannot block the fault current while the fault-blocking SMs can produce negative voltages against the ac-side voltages so that the fault current can be blocked.

To accurately investigate the internal dynamics of the MMCs, all capacitor voltages should be considered to evaluate the applied control strategies. This detailed ECM is solved by calculating all SM capacitor voltages to estimate each arm voltage. The detailed ECM needs capacitor voltage balancing strategy and is applicable for evaluating the performance of the practical control algorithms, e.g., power flow control, capacitor voltage balancing, circulating current control, and startup control. To further improve the computational efficiency of modeling and simulating large-scale MMC-based hybrid ac and dc systems, the proposed ECM can be modified by reducing the number of state variables, i.e., capacitor voltages. This reduced-order ECM assumes that all capacitor voltages are well balanced and only the average capacitor voltage of each arm is considered to calculate the arm voltage.

Performance Evaluation and Verifications

To verify the proposed ECM, a point-to-point MMC-HVDC system is selected as the study system and built in PSCAD/EMTDC program environment. Various MMC configurations based on different SM circuits are modeled and simulated under different operating conditions to evaluate the performance of the proposed modeling technique. The simulation results show that the proposed ECM can accurately and efficiently model and simulate the MMC-based systems for various SM circuits and arm configurations under different operating conditions. For the study cases, the simulation run time can be reduced from several or tens of thousands seconds to tens of seconds. With the conventional DSM, the SMs with more complex circuit topology have longer runtime. However, by using the proposed ECM, the run time is not related to the circuit topology complexity. The run time is determined by the number of voltage levels. For the proposed reduced-order ECM, there is no significant increase in run time when the voltage level is low. In addition, the STATCOM mode under dc fault condition can be implemented based on the proposed ECM.

Conclusions

- The proposed ECM can significantly improve simulation efficiency (speed) while keeping enough accuracy.
- The complexity of SM circuit topology significantly influences the simulation run time for the conventional detailed switching model. However, there is no significant impact of SM circuit topology on the run time of the proposed ECM.
- The run time of the proposed ECM increases with the increasing number of voltage levels.

Project Publications:

- [1] L. Zhang, J. Qin, D. Shi, and Z. Wang, "Efficient modeling of hybrid MMCs for HVDC systems," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 1629-1633.
- [2] L. Zhang, J. Qin, D. Shi, and Z. Wang, "An Improved Equivalent Circuit Model of MMC and Influence Analysis of Simulation Time Step," *IEEE Transactions on Power Delivery*, in preparation.

Student Theses:

- [1] Lei Zhang. *Modeling and Control of Modular Multilevel Converters for High-Power Applications*. PhD dissertation, Arizona State University, Tempe AZ, expected in January 2020.