G. Heydt, D. S. James, E. Gel, M. Albu, N. Hubele, "The reliability analysis of high power switches composed of series and parallel branches," paper 03GM0052, IEEE Power Engineering Society General Meeting, July 2003, Toronto, Ontario.

The Reliability Analysis of High Power Switches Composed of Series and Parallel Branches

G. T. Heydt[1] *Fellow*
D. S. James[1] *Student Member*
E. S. Gel[3] *Non-Member*
M. M. Albu[2] *Member*
N. F. Hubele[3] *Senior Member*

1 Department of Electrical Engineering 2 Fullbright Fellow on leave from the Politehnica Bucuresti, Bucharest, Romania
3 Department of Industrial Engineering

Arizona State University
Tempe, AZ

Abstract

This paper contains an analytical method for the failure analysis of a matrix configuration of switches in series and parallel. The concept is to use lower voltage and current rating switches in series and parallel to attain the higher ratings needed in power engineering applications. The analysis is based on probability state transition. A discussion of voltage and current snubbing is given. Representative results are illustrated and applications are suggested.

Index terms: Circuit breaker; switches; reliability; failure modes.

I. Introduction

IT IS NOT unusual in power engineering to attain high power ratings through the use of many components of lower rating. These components may be connected in series and parallel to obtain higher voltage and current ratings. For example, for the case of the application of switches with voltage and current rating V and I, if N_{se} switches are connected in a series string, and N_{pl} parallel strings are utilized, the resultant $N_{se}N_{pl} = N$ switches will have an equivalent rating of $N_{se}V$, $N_{pl}I$. The term *string* as used here refers to a series connection of several switches. Through the use of series and parallel connections, it is possible to utilize lower voltage and current rated switches to build up a high rating switch (e.g., for power engineering applications): this concept applies to mechanical switches as well as electronic switches. The basic concept is shown in Figure 1.

The reliability of series and parallel components has been discussed in many contexts, including power engineering. Billinton gives the basic formulation [1] and applications of series and parallel transmission components are discussed. References [2-5] give additional applications in a range of areas, including industrial engineering.

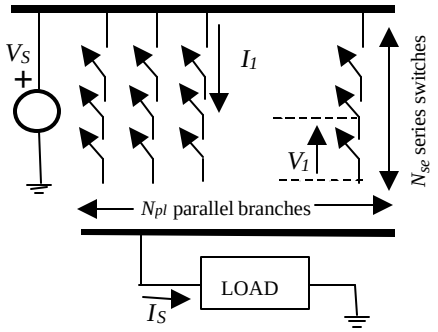

Fig. 1 Series and parallel combination of switches

In Figure 1, V_1 and I_1 denote the single switch voltage and current. Perfect voltage and current grading is assumed. The probability of failure of a switch is a function of the single switch voltage and current. Although the physical process is complex, it is reasonable to assume that the probability of failure of a switch with applied voltage V and applied current I is q_{VI} as shown pictorially in Figure 2. The shape of the probability of failure curve is dependant on additional factors such as the number of switch operations (as well as other factors of age and operating history), whether the switch has been exposed to high current switching (or only zero current switching known as *cold switching*), the switch type, and characteristics of $v_1(t)$ and $i_1(t)$. For simplicity of analysis of the basic structure of failure, it is assumed below that failure of an entire series switch is in the shorted mode; and failure of a series string is the dual phenomenon or failure in the open mode. In this ideal analysis, it is assumed that the voltage grading is such that series connected switches have equal individual impressed voltage; and parallel strings share current equally. Neither on-resistance nor off-resistance of the switch is modeled at this point (although resistance shall be modeled in simulations discussed later).

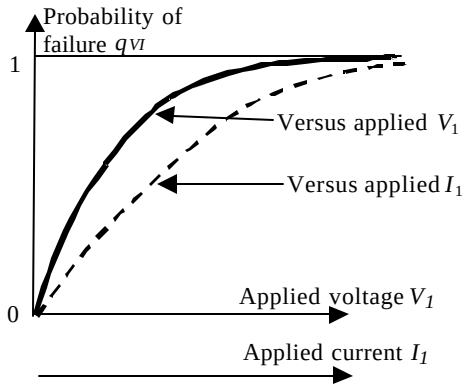

Fig. 2 Pictorial of the probability of failure, q, of a single switch versus applied voltage and current. Voltage and current scales are omitted for this pictorial

II. The state transition diagram

A widely used method of analysis for failure analysis is based on the use of a state transition diagram. Figure 3, for example, shows several possible states of operation of a multi-component system. State 1 denotes sub-component 1 operative, subcomponent 2 operative … subcomponent N operative. State 2 represents all subcomponents operative except for unit N which has failed; state 3 represents all operative except for unit N-1; …; and state 2^N represents operation with all subcomponents failed. In Fig. 3, branch probabilities are labeled for a two by two matrix of switches as an illustration.

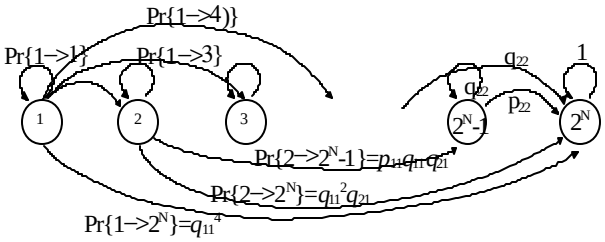

Fig. 3 State transition diagrams with representative states and branches indicated. The probability associated with branches is indicated for selected elements for a two by two switch matrix illustration.

The several branches depicted in Figure 3 represent the conditional probability of transitioning to another state given the present system state. The lower case notation p_{VI} is used to represent the probability of a successful switching operation (without failure) and q_{VI} (as shown in Fig. 2) is 1- p_{VI}. In Fig. 3, note that multiple switch failures at any one instant is possible and is modeled. In Fig. 3, the notation $\Pr\{a \rightarrow b\}$ refers to the probability of transitioning from state a to state b. This type of model is a Markov chain model and it is assumed that the branch probabilities are a function only of the branch terminal states. Also, it is assumed that the probability of failure of a switch is not a function of the switch status (i.e., ON or OFF).

Consider a probability vector P with 2^N rows, each of which represents the probability of residing in that operating state. Let P_n denote the probability vector at time n, and let P_o be the vector $[1 \;\; 0 \;\; 0 \;\; \ldots \;\; 0]^T$. Then

$$P_{n+1} = A\,P_n \qquad (1)$$

where A is a state transition matrix whose elements are the branch probabilities depicted in Figure 3. Although the elements of A are functions of the single switch voltage and current, within the designated probability states, V_1 and I_1 are fixed. Therefore (1) is a linear difference equation. The solution is simply

$$P_n = A^n\,P_o. \qquad (2)$$

As $n \rightarrow \infty$, P_n goes to $[0 \;\; 0 \;\; 0 \;\; \ldots \;\; 0 \;\; 1]^T$ (i.e., all switches fail in the limit).

It is possible to order the states in such a way that

- All switches operating is first (Tier 0)
- One switch failed is states 2 through N+1 (Tier 1)
- Two switches failed is states N+2 through N+1+$_2C_N$ (Tier 2). Note that the notation $_iC_j$ denotes the combinatorial

$$_iC_j = \frac{i!}{(i-j)!\,j!}.$$

- The state that k switches have failed corresponds to states numbered 1+ $_oC_n$ + … + $_{k-1}C_N$ through $_oC_N$ + … + $_kC_N$ (in Tier k)
- All switches failed is the last state numbered 2^N (Tier N).

The entire array is considered as failed if the system has reached state 2^N. Under some circumstances it may be advisable to modify this failure criterion to the following: the array is considered to have failed if either the number of series connected switches in any one string drops below $N_{se,min}$ or the number of operative parallel branches drops below $N_{pl,\,min}$. For purposes of the simplified ideal analysis, the former criterion is used, although it is not complex to extend the failure criterion to the latter.

The denomination of the *tiers* of states is such that when the circuit operates in Tier i, transition is possible only to the present operating state or to a successive (lower) tier (i.e., i+1, i+2, …, 2^N). This fact gives a special structure to the state transition matrix A. The general form of A is shown in Figure 4. Some points to note in the structure include:

- The matrix partitions correspond to the tiers.

- The first tier can transition to all other tiers. In general, tier i contains all zero entries except to the right of the principal diagonal, and the diagonal itself.
- The block submatrices along the principal diagonal are diagonal matrices.
- The row sum of all rows of A is unity.

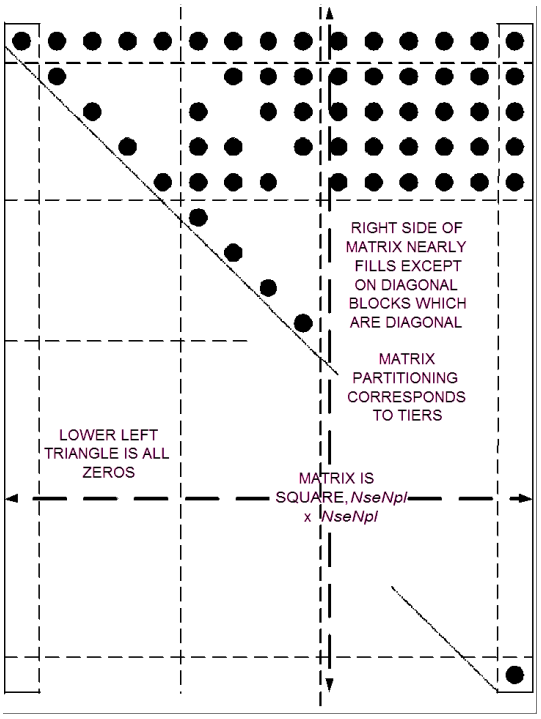

Fig. 4 Special structure of the state transition matrix A for series and parallel connected switches

III. Reliability calculations

The following questions are of particular interest:

(1) What is the distribution of lifetime for a system that starts with all switches functional, i.e., initial state of (11…1)?

(2) What is the expected lifetime for the system?

(3) For each switching epoch, what is the probability that the system is nonfunctional?

To answer the first two questions, define $f_{ij}^{(n)}$ which denotes the probability that the first passage time from state i to j (the first time step at which the system visits state j after visiting state i) is equal to n. It is easy to calculate $f_{ij}^{(n)}$ for each state and n, by using the following recursive relationship,

$$f_{ij}^{(m)} = \sum_{k \neq j} p_{ik} f_{kj}^{(m-1)}$$

where p_{ij} denotes the one-step transition probability from state i to j. Since the state (00…0) is absorbing, the probability distribution of the first passage times from state (11…1) to state (00…0) gives the distribution of the system lifetime.

Below consider the distribution of the system lifetime as a function of number of steps. For the example below, the failure probabilities are selected as

$q_{11} = 1 - p_{11} = 0.0001$ $\quad q_{21} = 1 - p_{21} = 0.0004$

$q_{12} = 1 - p_{12} = 0.0004$ $\quad q_{22} = 1 - p_{22} = 0.0008$

This assignment assumes that the affects of increased voltage and current are identical. For this case, the expected lifetime is 6664 steps or switching operations. Figure 5 shows the distribution of the lifetime.

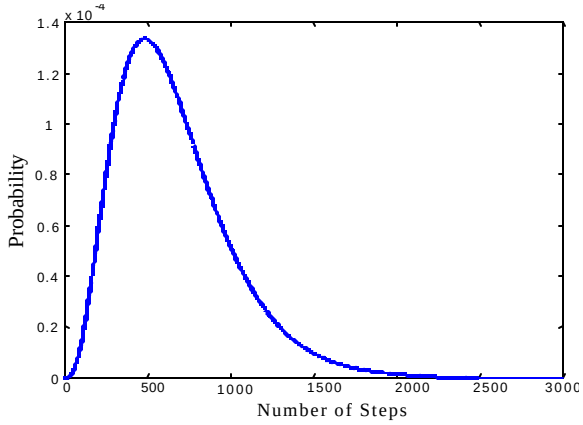

Fig. 5 Probability distribution of the lifetime of a matrix of series / parallel switches

The probabilities of very long and very short first passage times are low. As the system survives through switching operations, and the number of steps that the system has survived increases, the already failed switches accelerate the system failure, decreasing the probability of longer lifetimes.

To answer the third question, calculate P_i as defined in Equation (2). These probabilities represent the probability of finding the system nonfunctional before the n^{th} switching operation. The following illustration shows P_i as a function of the number of steps, n. The P_n approaches 1 in the last row, which means that as the number of steps or switching operations increases, the probability that system is nonfunctional at the next switching operation approaches to 1. This is an obvious result of the fact that state (00…0), which indicates a nonfunctional system, is absorbing.

To illustrate the calculation capability of the Markov analysis of switch failures for a series / parallel array, consider the case of a two by two array (N_{se} = 2, N_{pl} = 2) with different failure probabilities from the illustration above. Although this example is small, it is useful to illustrate the concept. For the illustration, let the degradation of switch failure rate with voltage be exponential, and the degradation of failure rate with the switched current be linear. These rate

characteristics are not suggested on the basis of measurements nor experience; instead the failure rates are used for illustration only. For the illustration, the source voltage is assumed to be 480 Vdc and the load current is 100 mA. The probability of switch failure with 240 V (graded) across each switch and 50 mA in each switch (i.e., all switches operational) is 0.9999 As series components fail, the applied voltage across each switch is 480 V and the probability of failure drops to 0.999 As series strings are removed from service the probability of failure drops from 0.8 to 0.7 For this example, the probability of failure versus number of switch operations is shown in Fig. 6. The figure depicts the last row of vector P in (2) versus n. Of course, as $n \to \infty$, P_n goes to $[0 \quad 0 \quad 0 \quad \ldots 0 \quad 1]^T$ and the probability of failure goes to unity. For purposes of this illustration, the definition of switch matrix failure is taken to be the state (00…0) (i.e., all switches failed).

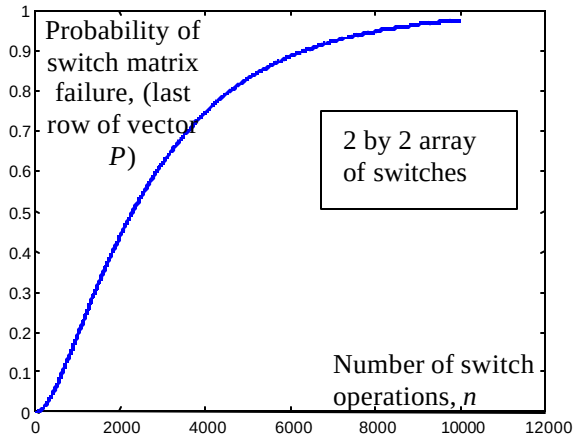

Fig. 6 Probability of switch failure versus number of operations for an illustrative 480 V, 100 mA switch matrix

A large variety of studies can be done to evaluate the overall switch matrix performance: as a further illustration, the probability of switch matrix failure versus individual switch probability of failure can be assessed. Figure 7 shows the expected number of switch operations to obtain probability of switch matrix failure of 0.5 The figure is drawn versus the probability of failure of *one* switch at voltages V_1 = 240 and 480 respectively as {0.99, 0.9}, {0.999, 0.99}, …, {0.9999, 0.999}. The vertical axis in Figure 7 does not directly indicate the number of switch operations to failure.

IV. Grading and snubbing

The foregoing concept of series and parallel circuits requires some practical considerations in real applications. In order to render the voltage across individual switches in a series string to be the same, voltage grading is needed. In switching applications, a wide variety of electrical components can be used to break electric currents. Some of these include mechanical switches, MEMS, thyristors, IGBTs, and SCRs which are all chosen depending upon the voltage, and current ratings of the switch. In power applications, inductive loads will often produce high switch voltages and currents during the turn-on and turn-off periods. Snubber circuits are often used to protect the switches and to 'reshape' the transients by dissipating energy into snubber components. Snubbers are often designed to perform the following functions [6]:

- Peak voltage limiters (during turn-on)
- Rate of rise (*dv/dt*) voltage limiters
- Peak current limiters (during turn-off)
- Rate of rise (*di/dt*) current limiters.

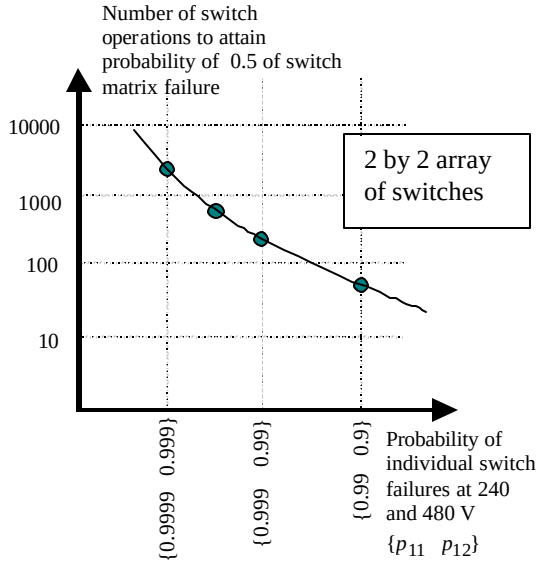

Fig. 7 An illustration of the calculation capability of the Markov chain approach: the number of expected switch operations to attain probability 0.5 of the failure of the switch matrix versus the probability of individual switch failure (represented as $\{p_{11} \quad p_{12}\}$ which is the probability of failure for V_1 = 240 and 480 V respectively). Note the log-log scale and pictorial scale on horizontal axis.

Voltage grading is accomplished using a series resistor string of high resistance with junctions between the resistors connected to the junction points of series connected switches. This is a common practice in high voltage engineering. Current grading is accomplished by applying a series conductance in each series string.

Because the snubber requirements are more complex than the voltage and current grading requirements, attention focuses on the required snubbers. The function of the turn-off snubber is to limit the peak voltage across the switch during the opening

period, $t_{s(turn-off)}$. An example of a turn-off snubber (or overvoltage snubber) is depicted in the RCD ('resistor - capacitor - diode') circuits of Fig. 8. Figs. 8 (a-b) show the current paths through the RCD snubber during the turn-off switching period. During this phase, the diode shorts the resistive component, R_S, and allows the capacitor to charge where $V_{CS} \approx V_S$ (neglecting diode voltage). In this transition period, Δt_S, the charging of the capacitor 'relieves' the electrical stress on the switch and creates a softer turn-off voltage on the switch. Alternatively, Figs. 8 (c-d) depict the RCD snubber during the turn-on period, $t_{s(turn-on)}$. The charged capacitor dissipates its energy into the snubber resistor, R_S, assuming the on-state resistance of the switch is substantially smaller than its snubber counterpart or $R_S >> R_{switch-on}$. With this assumed, the power dissipated by the snubber can be evaluated as

$$P_{R_s} = \frac{C_S V_S^2}{2} \qquad P_{R_s(peak)} = \frac{V_S^2}{R_S} \ .$$

As seen in Fig. 9, the transient voltage across the switch during the time of switch opening is reduced by the addition of the RCD snubber.

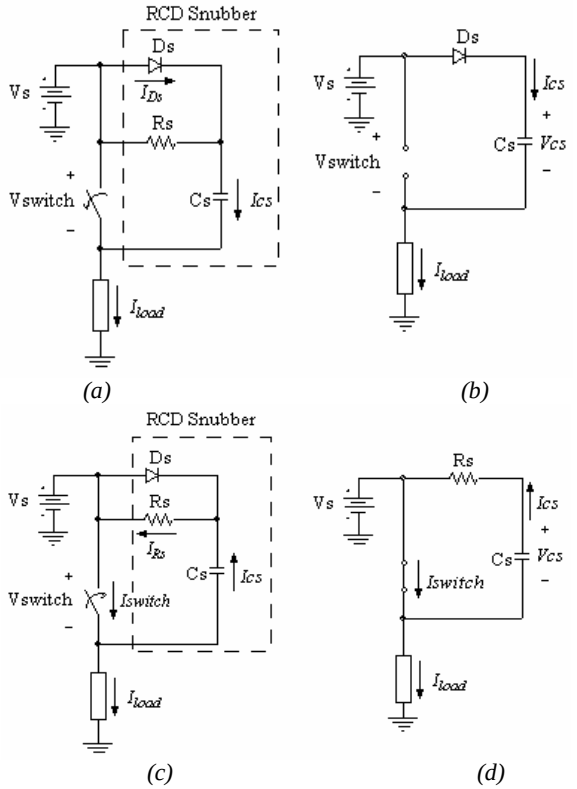

Fig. 8 Various stages of snubber operation: (a) turn-off RCD snubber at $t = t_{s\ (turn-off)}$ (b) equivalent circuit during turn-off period (c) turn-off RCD snubber at $t = t_{s\ (turn-on)}$ (d) equivalent circuit during turn-on period

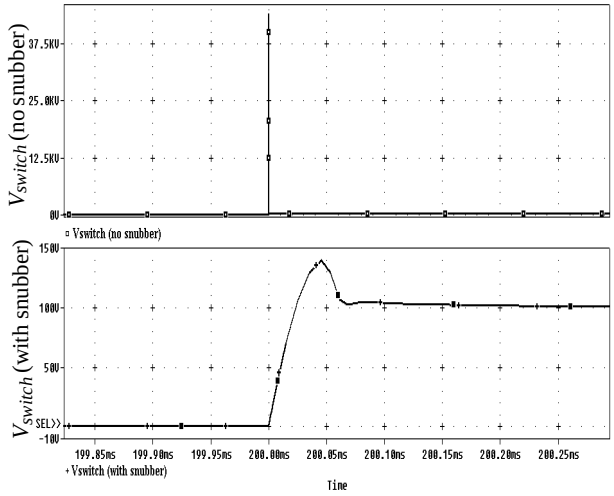

Fig. 9 Simulated voltage spike of unprotected and protected switches R_s = 5 kΩ, C_s = 10 nF, $t_{s(turn-off)}$ = 0.1 *ms*

The turn-on snubber aids in regulating the amount of current through the switch at the moment of closing. At $t = t_{s(turn-on)}$, the inductor provides a 'soft-start' in delivering current to the load. This is especially helpful in non-inductive loads to alleviate the instantaneous current through the switch. At switch opening, the current through the snubber inductor can cause additional voltage stresses on the switch as seen in Fig. 10. The terminology *RLD* refers to a snubber composed of a resistor, inductor, and a diode.

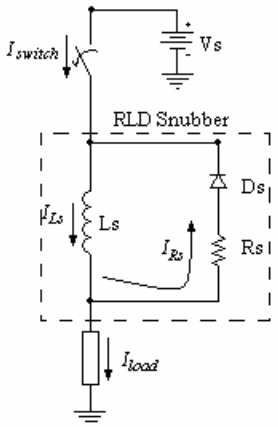

Fig. 10 Turn-on RLD snubber (at $t = t_{s(turn-off)}$)

In addition to regulating transients in a switch, snubbers can be used in voltage and current grading techniques. Fig. 11 depicts an N_{se} *x* N_{pl} configuration of switches in series and parallel with RCD voltage snubbers. During the switching transients and

steady-state operating modes, the snubbers ensure an equal distribution of voltage and current is provided to each switch.

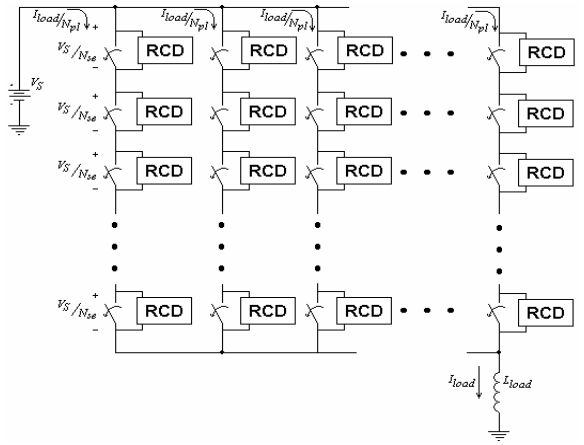

Fig. 11 N_{se} x N_{pl} configuration of switches with RCD snubbers

Assuming identical and ideal components, the voltages and currents are equal for every switch and parallel string.

$$V_{switch} = \frac{V_s}{N_{se}} \qquad I_{switch} = \frac{I_{load}}{N_{pl}}$$

The total power absorbed by the snubber system is equal to

$$P_{s(mxn)} = N_{se} N_{pl} \left(\frac{C_s V_s^2}{2} \right).$$

V. Application areas

The application of series and parallel elements is widespread: many semiconductor components are rated at low voltage and/or low current, and these components can be configured in series and parallel for realistic power engineering applications. Mechanical switches may also be placed in series and parallel to attain higher effective ratings. The present work is part of a larger research effort in which micromechanical switches (MEMS) are being considered for power switching.

Perhaps the most intriguing application is the use of the indicated technology to determine where additional investment is to be made in series and parallel topologies. The probability state transition approach may be used to design the number of series and parallel branches in order to attain a given level of reliability. Also, it is possible to determine whether N_{se} or N_{pl} is to be increased to obtain an optimum increase in reliability. Although no actual designs have been done using the proposed methodology, the simulation studies and results indicate that the method is practical for the detailed failure analysis of series and parallel topologies.

As an illustration, a 3 x 4 multiple switch configuration with RCD snubber protection circuit (see Fig. 8) was simulated with PSpice. Table 1 includes a list of parameters for the sample simulation illustrated below. Ideal switching is assumed which includes:

- Synchronized switching among all components
- Minimal switching transition periods
- Minimal on-state switch resistance
- Maximum off-state switch resistance
- Ideal voltage source (no internal impedances)
- RL load

Table 1 RCD Snubber circuit simulation parameters

DC Voltage, Vs	100 V
Load Current, Is	50 mA
Snubber Capacitance, Cs	10 nF
Snubber Resistance, Rs	5 kΩ
Load Resistance	2 kΩ
Load Inductance	50 mH
On-State Switch Resistance, R_{on}	0.1 mΩ
On-State Switch Resistance, *Roff*	1 MΩ
Switch opening time, $\Delta t_{s(turn-off)}$	0.1 ms
Switch closing time, $\Delta t_{s(turn-on)}$	0.1 ms

The results of the turn-off period (see Table 2) show that even with a large system of switches, the voltages and currents are distributed evenly among the switches. The switch overvoltages at $t = t_{s(turn-off)}$ are similar to those found in the single switch operations. The turn-on and turn-off times, $\Delta t_{s(turn-on)}$ and $\Delta t_{s(turn-off)}$ were calculated as

$$\frac{\left| I_{load(nom)} - I_{load(settled)} \right|}{I_{load(nom)}} = 3\% \quad \text{at} \quad t = t_{s(turn-on)}$$

and

$$\frac{\left| V_{switch(nom)} - V_{switch(settled)} \right|}{V_{switch(nom)}} = 3\% \text{ at } t = t_{s(turn-off)}.$$

Figs. 12 - 13 show typical results.

Table 2 Sample simulation results for series and parallel switch topologies

Results for switch turn-off		Results for switch turn-on	
$V_{switch(peak)}$	139.5 V	V_{switch}	100 V
$V_{switch(nom)}$	100 V	$\Delta t_{s(turn-on)}$	0.2 ms
$\Delta t_{s(turn-off)}$	0.2 ms	$P_{R_s(peak)}$	2 W
I_{c_s}	50 mA	I_{c_s}	50 mA

V_{C_S}	100 V	V_{C_S}	100 V

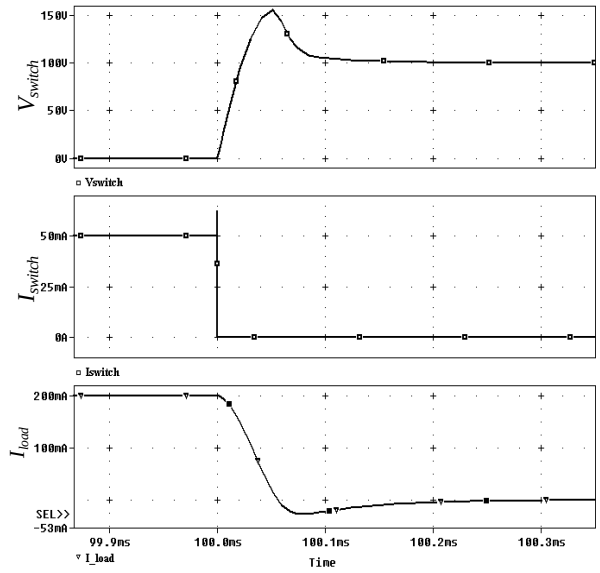

Fig. 12 Simulated waveforms of 3 x 4 switch with RCD snubbers in turn-off period

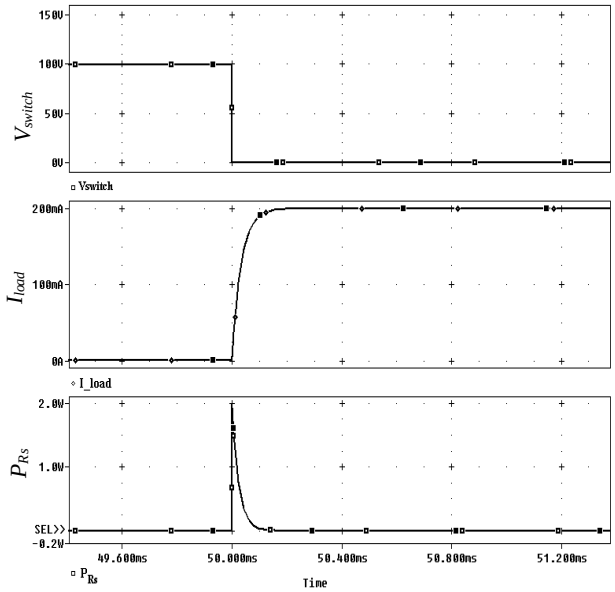

Fig. 13 Simulated waveforms of 3 x 4 switch with RCD snubbers in turn-on period

In coordination with the voltage and current regulation, switch reliability is maximized by the proper selection of R_S and C_S. To test the robustness of the RCD snubber, a series of evaluations was performed with varying values of R_S and C_S. The tested values included ranges $10\,\Omega < R_S < 10\,\mathrm{k}\Omega$ and $0.1\,nF < C_S < 10\,mF$. The system responded independently of the varying values of R_S. The only control evident was the peak power of the snubber resistor. As seen in Fig. 14, the settling time of the load current, I_{load} is dependent of the snubber capacitance, C_S.

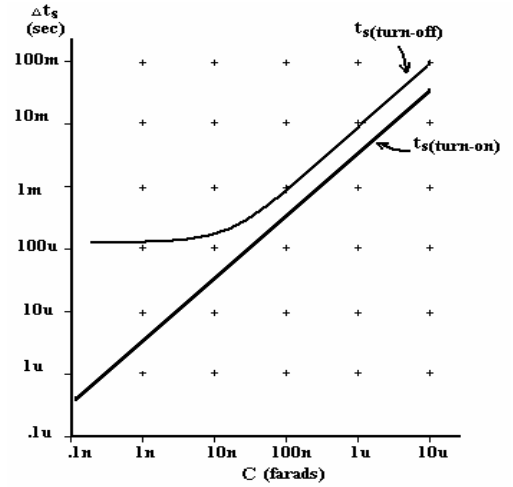

Fig. 14 Δt_S vs. C_S for 3 x 4 switch with RCD snubber

When connecting the switches and snubbers into an N_{se} x N_{pl} array, two distinct topologies arise: the isolated string method or the cross-bridge method. The isolated string method in Fig. 15 connects each individual string (or column) into separate feeds from the voltage source to the node. The currents from each string conjoin at the load node, but the switch voltages are isolated from string to string. The cross-bridge method interconnects switches of common rows (Fig. 16) allowing horizontal current flow between strings. Table 3 contains a brief analysis of the two topologies.

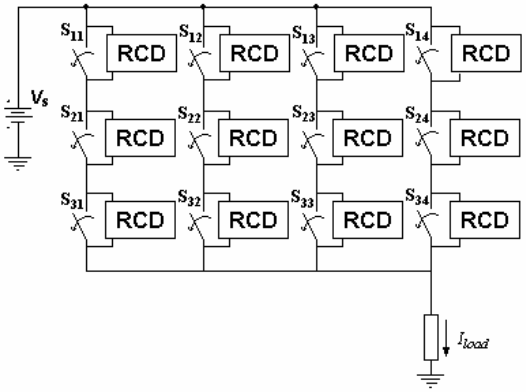

Fig. 15 Switch series / parallel array: isolated string method

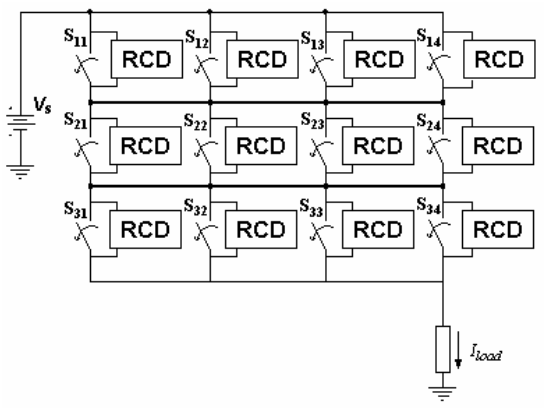

Fig. 16 Switch series / parallel array: cross bridge method

Table 3 Analysis of system response to switch failures

Configuration	Failure mode	V_1	I_1
Cross bridge	Short Circuit	V_1 increases by $\frac{V_s N_{se}}{N_{se}-1}$ for switches in different rows	Unaffected for all switches outside failed row
	Open Circuit	V_1 unaffected for all switches	I_{switch} increases by $\frac{I_{load} N_{pl}}{N_{pl}-1}$ for switches in the same row
Isolated string	Short Circuit	V_{switch} increases $\frac{V_s N_{se}}{N_{se}-1}$ by for switches in same column	Unaffected for all switches
	Open Circuit	V_{switch} unaffected for all switches	I_{switch} increases by $\frac{I_{load} N_{pl}}{N_{pl}-1}$ for switches in the different columns

VI. Conclusions

The main conclusion of the paper is that it is possible to assemble low rating switches in series and parallel for higher rating applications. It is necessary to utilize voltage and current snubbing for this application. An RCD snubber is suggested for a voltage snubber. Voltage and current grading are also required. The failure analysis of this matrix configuration is possible using a Markov chain. The model permits the calculation of the probability of failure versus time using (2). The influence of individual switch failure characteristics on the overall probability of failure is illustrated thereby allowing the evaluation of need for redundancy. A distinctive structure of the state transition matrix, *A*, for this application is demonstrated.

References

[1] R. Billinton, Power System Reliability Evaluation, Gordon and Breach, New York, 1970.

[2] Y-H. Chung, "Medium Voltage Hybrid Transfer Switch," Proc. IEEE Power Engineering Society Winter Meeting, January 2002, v. 2, pp. 1158 -1163.

[3] G. Chaudhuri, K. Hu, N. Afshar, "A New Approach to System Reliability," IEEE Trans. on Reliability, v. 50, No. 1, March 2001, pp. 75 - 84.

[4] M. Moustafa, "Reliability Model of Series-Parallel Systems," Microelectronics and Reliability, v. 34, No. 11, Nov, 1994, pp. 1821-1823.

[5] A. Lesanovsky, "Systems With Two Dual Failure Modes - A Survey," Microelectronics and Reliability, v. 33, No. 10, Aug, 1993, pp. 1597-1626.

[6] N. Mohan, T. Undeland, W. Robbins, Power Electronics, John Wiley and Sons, New York, 1995.

Acknowledgements

The authors acknowledge the technical input and suggestions of their colleagues Drs. G. Karady, and B. Kim. The work is supported by the National Science Foundation / United States Department of Defense program "Electric Power Networks Efficiency and Security" under contract ECS-0224228.

Biographies

Gerald Thomas Heydt is from Las Vegas, NV. He holds the Ph.D. in Electrical Engineering from Purdue University. He is a member of the National Academy of Engineering. Dr. Heydt is presently the director of a power engineering center program at Arizona State University in Tempe, AZ.

Daniel Scott James is from Granite City, Illinois. Mr. James holds the BS degree from Southern Illinois University - Edwardsville. He is presently working toward the MSEE degree at Arizona State University.

Esma Senturk Gel is from Istanbul, Turkey. She holds the PhD in Industrial Engineering from Northwestern University. Dr. Gel is presently an Assistant Professor of Industrial Engineering at Arizona State University. She is interested in stochastic modeling and control.

Mihaela Marilena Albu is from Craiova, Romania. Dr. Albu holds the PhD degree from the Universitatea Politehnica Bucuresti. She is presently a Professor of Electrical Engineering at the same university. Dr. Albu is spending a leave at Arizona State University as a Fullbright Fellow 2002 - 03.

Norma F. Hubele is a Professor of Industrial Engineering. Dr. Hubele received the PhD degree in Industrial Engineering from Rensselaer Polytechnic Institute.